Scheme & Syllabus

For

Master of Technology

(Electronics & Communication Engineering)

w.e.f.

2022-23

Department of Electronics & Communication Engg.

Guru Jambheshwar University of Science & Technology
HISAR-125001, Haryana

M.Tech (ECE)

Program Outcomes and Program Specific Outcomes

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PSO1: Students should be able to develop advanced understanding of the concepts of Electronics & communication engineering and their applications in the specific areas of VLSI, Communication Engineering and signal processing.

PSO2: Students should have an ability to apply technical knowledge of modern hardware & software tools for the design of electronic subsystems for solving various engineering problems.

Semester	Total Credits
I	26
II	22
III	14
IV	08
Total	70

- 04 contact hours per week are required for each theory subject including electives. However, 03 contact hours per week are required for open elective subject.
- 04 contact hours per week are required for each laboratory course.
- 02 hrs per student per week teaching load will be assigned to supervisor for dissertation work for Part I and Part II each.

M. Tech. (ECE), 1st Semester										
Sr. No.	**Course Code**	**Course Title**	**Teaching Schedule (Hrs/week)**			**Credit**	**Exam Duration (Hr)**	**Internal Marks**	**External Marks**	**Total Marks**
			L	**T**	**P**					
1	ECL-712	IC Fabrication Technology	4	0	0	4	3	30	70	100
2	ECL-713	Digital VLSI Design	4	0	0	4	3	30	70	100
3	ECL-714	Hardware Description Language	4	0	0	4	3	30	70	100
4	ECL-715	Embedded System Design	4	0	0	4	3	30	70	100
5	ECL-719	Signal Processing	4	0	0	4	3	30	70	100
6	ECP-716	Digital VLSI Design Lab	0	0	4	2	3	50	50	100
7	ECP-717	Hardware Description Language Lab	0	0	4	2	3	50	50	100
8	ECP-718	Embedded System Design Lab	0	0	4	2	3	50	50	100
9	ACXX	Audit Course*	2	0	0	0	3	30	70	100
		Total	**22**	**0**	**12**	**26**		**300**	**500**	**800**

***List of Audit Course (1st Semester)**

The student can opt for any one subject from the following list.

Sr. No.	Course Code	Course Title
1	AC01	English For Research Paper Writing
2	AC02	Disaster Management
3	AC04	Value Education
4	AC07	Stress Management By Yoga

M. Tech. (ECE), 2nd Semester										
Sr. No.	**Course Code**	**Course Title**	**Teaching Schedule (Hrs/week)**			**Credit**	**Exam Duration (Hr)**	**Internal Marks**	**External Marks**	**Total Marks**
			L	**T**	**P**					
1	ECL-721	Mobile Communication	4	0	0	4	3	30	70	100
2	ECL-722	Advance Optical Communication System	4	0	0	4	3	30	70	100
3	ECL-723	Analog IC Design	4	0	0	4	3	30	70	100
4	ECL-724	Adaptive Signal Processing	4	0	0	4	3	30	70	100
5	ECL-725	Elective-I*	4	0	0	4	3	30	70	100
6	ECP-726	Adaptive Signal Processing Lab	0	0	4	2	3	50	50	100
7	ACXX	Audit Course*	2	0	0	0	3	30	70	100
		Total	**22**	**0**	**04**	**22**		**200**	**400**	**600**

***List of Elective-I (2nd Semester)**

The student can opt for any one subject from the following list.

Sr. No.	Course Code	Course Title
1	ECL-725(i)	Algorithm for VLSI Design Automation
2	ECL-725(ii)	Advanced Computer Architectures
3	ECL-725(iii)	MEMS and IC Integration
4	ECL-725(iv)	Organic Semiconductors
5	ECL-725(v)	Artificial Intelligence

***List of Audit Course (2nd Semester)**

The student can opt for any one subject from the following list.

Sr. No.	Course Code	Course Title
1	AC03	Sanskrit For Technical Knowledge
2	AC05	Constitution of India
3	AC06	Pedagogy Studies
4	AC08	Personality Development Through Life Enlightenment Skills

M. Tech. (ECE), 3rd Semester										
Sr. No.	**Course Code**	**Course Title**	**Teaching Schedule (Hrs/week)**			**Credit**	**Exam Duration (Hr)**	**Internal Marks**	**External Marks**	**Total Marks**
			L	**T**	**P**					
1	ECL-731(x)	Elective-II	3	0	0	3	3	30	70	100
2	3OExx	Elective-III (Open Elective)	3	0	0	3	3	30	70	100
3	ECP-732	Advance VLSI Design Lab	0	0	4	2	3	50	50	100
4	ECP-733	Communication System Design Lab	0	0	4	2	3	50	50	100
5	ECD-730	Dissertation-Part I	0	0	*	3	-	100	-	100
6	ECP-735	Seminar	0	0	2	1	-	100	-	100
		Total	**6**	**0**	**10**	**14**		**360**	**240**	**600**

*02 hrs per student per week teaching load will be assigned to supervisor for Dissertation - Part I.

List of Elective-II (3rd Semester)

The student can opt for any one subject from the following list.

Sr. No.	Course Code	Course Title
1	ECL-731(i)	Mixed Signal Design
2	ECL-731(ii)	RF Micro-electronics
3	ECL-731(iii)	VLSI Testing and Testability
4	ECL-731(iv)	Memory System Design
5	ECL-731(v)	Low Power VLSI Design
6	ECL-731(vi)	Wireless Sensor Networks
7	ECL-731(vii)	Advanced Digital Communication
8	ECL-731(viii)	Satellite Communication

9	ECL-731(ix)	FPGA Design
10	ECL-731(x)	Advanced Antenna Theory and Design

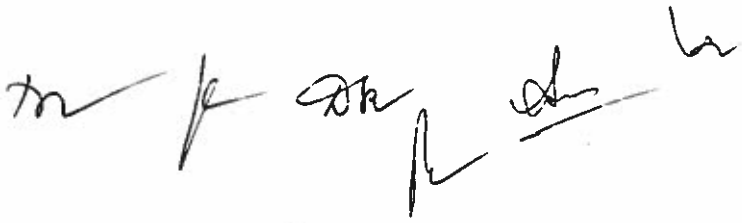
List of Elective-III (Open Electives)

Separate list of Open Electives (Elective-III) is to be provided by the Dean, FET.

M. Tech. (ECE), 4th Semester										
Sr. No.	**Course Code**	**Course Title**	**Teaching Schedule (Hrs/week)**			**Credit**	**Exam Duration (Hr)**	**Internal Marks**	**External Marks**	**Total Marks**
			L	**T**	**P**					
1	ECD-740	Dissertation-Part II	0	0	*	8	-	-	100	100
		Total	**0**	**0**	**-**	**8**		**-**	**100**	**100**

*02 hrs per student per week teaching load will be assigned to supervisor for Dissertation - Part II.

First Semester



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IC Fabrication Technology
ECL-712

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Analog electronics, VLSI design

Course Objectives: This is the very first course for the post-graduate students. This course first gives the knowledge of the necessary environment conditions for the integration technology. All the fabrication processes are then discussed step-by step which includes wafer cleaning, wet etching, ion implantation, oxidation, lithography, chemical vapour deposition, metal film deposition, etching and then safe packaging.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Describe** basic terminology related to IC fabrication process.	LOTS: Level 1 Remember
CO 2	**Explain** various techniques such as oxidation, lithography, CVD technique etc.	LOTS: Level 2 Understand
CO 3	**Apply** knowledge of lithography, metallization and packing for ICs.	LOTS: Level 3 Apply
CO 4	**Evaluate** the lithography procedure and advanced lithography techniques used in the industry.	HOTS: Level 5 Evaluate
CO 5	**Design** integrated circuits in a better fashion with thorough knowledge of IC fabrication technique.	HOTS: Level 6 Create

UNIT-1

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology: Ion Implantation modelling, technology and damage annealing; characterization of Impurity profiles.

UNIT-2

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterizations of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

UNIT-3

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.

UNIT-4

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Reference Books:

1. S.K. Gandhi, "*VLSI Fabrication Principles*", Second Edition, John Wiley Inc. 1994.
2. S.M. Sze , "*VLSI Technology*", Second Edition, McGraw Hill, 1988.
3. Plummer. Deal, Griffin "*Silicon VLSI Technology: Fundamentals, Practice & Modeling*" Fifth Edition, Prentice Hall, 2001.
4. P. Van Zant, "*Microchip Fabrication*", Fifth Edition, McGraw Hill, 2000.
5. Gouranga Bose, "*IC Fabrication Technology*", First Edition, McGraw Hill, 2013.

Course Articulation Matrix:

IC Fabrication Technology (ECL-712)					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	L	--	M	H	M
CO 2	H	--	M	H	H
CO 3	L	L	H	H	H
CO 4	L	--	M	H	H
CO 5	H	--	H	M	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Digital VLSI Design
ECL-713

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Digital Electronics

Course Objectives: This course is intended to be used for the first year post- graduate students. This course aims at covering first the basic building block of the VLSI circuits, that is, MOSFET and then the design equations for MOS, transistor sizing, various logic circuits design using MOS transistor. Memory designs and layouts are also covered under this course.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO 1	**Describe** CMOS circuits and systems and their technical specifications and uses.	LOTS: Level 1 Remember
CO 2	**Explain** various CMOS technologies for logic gates, circuits and systems.	LOTS: Level 2 Understand
CO 3	**Apply** the concepts of CMOS logics for the design of digital integrated circuits and systems.	LOTS: Level 3 Apply
CO 4	**Analyze** CMOS static and dynamic circuits and systems.	HOTS: Level 4 Analyze
CO 5	**Evaluate** CMOS static and dynamic circuits.	HOTS: Level 5 Evaluate
CO 6	**Design** CMOS circuits and systems for digital IC design, test and verification.	HOTS: Level 6 Create

UNIT-1

Introduction to CMOS Technology: brief history, MOS transistors and switches, Design partitioning, Circuit and system representations examples, Design abstractions, design verification and testing. Technology related CAD issues. CMOS processing Technology- brief overview, CMOS technologies, Latch-up

UNIT- 2

MOS transistor theory: introduction, depletion and enhancement MOS transistor, MOS device design equations, current voltage (I-V) characteristics, Capacitance voltage (C-V) characteristics, second order effects, MOS models and small signal characteristics, Body Effect. CMOS inverter DC characteristics, static load MOS inverters, enhancement load versus depletion load inverter, CMOS inverter switching characteristics, power dissipation, charge sharing. Scaling of MOS transistors

UNIT- 3

CMOS logic gate design, logic fan-in, fan-out characteristics, Noise Margin, inverter device sizing, CMOS circuits-Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits. Sequential MOS Logic Circuits: SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop, set up and hold time, two phase clocking, clock distribution.

UNIT- 4

CMOS logic structures-CMOS complementary logic, pseudo –nMOS logic, dynamic logic, Clocked CMOS logic, CMOS domino logic, NP domino logic, cascade voltage switch logic,

memory elements, Finite state machines, CMOS testing- need, principles and design strategies for test-brief introduction.

Reference books:

1. Neil H. E. Weste, K. Eshraghian, *"Principles of CMOS VLSI Design: A Systems Perspective"*, Second Edition, AW/Pearson, 2001.
2. Neil H. E. Weste and David M Harris, *"CMOS VLSI Design· A Circuits and Systems Perspective"*, Fourth Edition, AW/Pearson, 2011.
3. S. M. Kang and Y. Leblebici, *"CMOS Digital Integrated Circuits: Analysis and Design"*, Third Edition, TMH, 2002.
4. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *"Digital Integrated Circuits: A Design Perspective"*, Second Edition, Pearson, 2003.
5. D. A. Pucknell and K. Eshraghian, *"Basic VLSI Design"*, Third Edition, PHI, 2001.

Course Articulation Matrix:

Digital VLSI Design (ECL-713)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	H	H	H	H
CO 2	H	H	H	H	M
CO 3	M	H	H	H	M
CO 4	M	H	M	H	M
CO 5	H	H	H	H	M
CO 6	H	H	H	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Hardware Description Language
ECL-714

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Digital Electronics

Course Objective: This course is for first year post graduation students. This course is designed to make students learn popular hardware descriptive languages such as Verilog & VHDL. The course begins with the introduction of Hardware design and Design Methodologies. Basic and advanced concepts required to write a Verilog code are covered in detail.

Course outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO 1	**Describe** the digital circuits and systems in Verilog with specifications for different applications.	LOTS: Level 1 Remember
CO 2	**Understand** behavioural, dataflow and Gate level modelling for digital logics and system implementation, testing of digital logic.	LOTS: Level 2 Understand
CO 3	**Apply** the concepts of Verilog HDL for digital logics design, synthesis, test and verification.	LOTS: Level 3 Apply
CO 4	**Analyze** the behaviour of digital circuits and systems using verilog.	HOTS: Level 4 Analyze
CO 5	**Evaluate** the behaviour of digital circuits and systems using verilog.	HOTS: Level 5 Evaluate
CO 6	**Design** different digital circuits and systems for digital IC design, test and verification with Verilog.	HOTS: Level 6 Create

UNIT-1

Digital system design automation with Verilog, digital design flow, Verilog HDL, Hierarchical Modeling Concepts, RTL design with Verilog, RTL level design, elements of Verilog, component description in Verilog, test bench, Verilog language concepts, characterizing hardware, module basics, Verilog simulation model, compiler directives, system tasks and functions

UNIT- 2

Combinational circuits description, module wire, gate level logic, hierarchical structure, assignment statements, behavioral combinational description, combinational synthesis

UNIT- 3

Sequential circuits description, sequential models, memory components, functional registers, state machines, sequential synthesis, Component test and verification, test bench, test bench techniques, design verification, assertion verification

UNIT- 4

Sequential multiplier, computer model, processor and memory model, data path part, control part, adding CPU Verilog description, CPU design and test

Reference books:

1. Z. Navabi, *"Verilog Digital System Design"*, Second Edition, McGraw Hill, 2015.
2. Samir Palnitkar, *"Verilog HDL-A Guide to Digital Design and Synthesis"*, Second Edition, SunSoft Press, 2001.
3. Stephen Brown and Zvonko Vranesic, *"Fundamental of Digital Logic with Verilog Design"*, Third Edition, McGraw Hill, 2014.
4. Charles H Roth (Jr.) and Larry L. Kinney, *"Fundamental of Logic Design"*, Sixth Edition, Cengage Learning, 2010.
5. Steve Kilts, *"Advanced FPGA Design-Architecture, Implementation, and Optimization"*, IEEE John Wiley & Sons, 2007
6. Hong Jeong, *"Architecture for Computer Vision-from Algorithm to Chip with Verilog"*, First Edition, John Wiley & Sons, 2014

Course Articulation Matrix:

Hardware Description Language (ECL-714)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	H	H	H	H
CO 2	H	H	H	H	H
CO 3	M	H	H	H	H
CO 4	M	H	M	H	M
CO 5	H	H	M	H	M
CO 6	M	H	M	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Embedded System Design
ECL-715

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Microprocessor, Basic of C language, Analog & Digital circuits

Course Objectives: This course is designed to impart in-depth knowledge related to the architecture and programming of PIC micro-controller. The course provides thorough coverage to advanced and state-of-the-art ARM based micro-controllers. Further it also familiarizes students with the concepts and techniques of embedded system project management.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able:	RBT Level
CO 1	**Outline** the architecture of PIC & ARM microcontroller.	LOTS: Level 1 Remember
CO 2	**Explain** various kinds of instruction sets of PIC & ARM microcontroller.	LOTS: Level 2 Understand
CO 3	**Apply** knowledge of architecture & instruction set in writing assembly language programs.	LOTS: Level 3 Apply
CO 4	**Analyze** various microcontroller based circuits.	HOTS: Level 4 Analyze
CO 5	**Design** and develop an embedded system for different applications.	HOTS: Level 6 Create

UNIT 1

Introduction to PIC Microcontrollers: Comparison between PIC16 (mid range 8 bits family) and PIC18 (advanced 8 bits family) families of microcontrollers.

PIC Architecture: Pin Diagram, Functional Block diagram, Program Memory Organization, Special Function Registers and Data Memory Organization, Architecture of Instructions: Bit oriented, Byte oriented, Literal and Control instructions.

UNIT 2

Timers & Interrupts in PIC: Timer 0 Module, Timer 0 as counter; Block Diagram of Timer1 Module; Timer1 as synchronous and Asynchronous counter; Timer1 Oscillator; Block Diagram of Timer2 Module; Interrupt logic diagram, Timer0 Interrupt, Port-B change Interrupt, RB0 Interrupt; Timer1 and Timer2 Interrupts and External interrupts, Interrupt Service Routine

Instruction set in PIC: Assembly Language Programming Style and Instruction set (PIC 16F877A), Introduction to IDEs for PIC programming, Simple Arithmetic operations; TRIS Registers of PORT A, B, C, D and E.

UNIT 3

ARM Architecture: The Acorn RISC Machine, Architectural inheritance, The ARM programmer's model, and ARM development tools.
ARM architecture variants, 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.

UNIT 4

Instruction Set of ARM: Introduction, Exceptions, Conditional execution , Branch and Branch with Link (B, BL), Branch with Link and exchange (BX, BLX), Software Interrupt (SWI), Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte instructions, Half-word and signed byte instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions.

Reference Books:

1. John B. Peatman, "*Design with PIC Microcontroller*", Second Edition, Pearson, 2002.
2. Steve Furber, "*ARM System-on-Chip Architecture*", Second Edition, Addison-Wesley, 2000.
3. Muhammad Ali Mazidi, "*PIC Microcontroller and Embedded Systems: using assembly and C for PIC 18*", First Edition, Pearson Education, 2008.
4. Muhammad Ali Mazidi, Sarmad Naimi, Sepehr Naimi, Shujen Chen, "*ARM Assembly Language Programming & Architecture*" Second Edition, Microdigitaled.com, 2016.
5. Saurabh chandrakar, "*Microcontroller & Embedded System Design*" First Edition, Dreamtech press & Wiley, 2019.

Course Articulation Matrix:

Embedded System Design (ECL-715)					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	H	--	M	H	M
CO 2	M	--	H	H	H
CO 3	H	L	H	H	H
CO 4	H	--	H	H	M
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Signal Processing

ECL-719

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Signal & System, Engineering Mathematics.

Course Objectives: To introduce the concepts and techniques associated with the understanding of signal processing. To familiarize with techniques suitable for auditory perception and time delay estimation. To provide with an appreciation of applications for system modeling and identification.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Describe** the terminologies used in speech processing.	LOTS: Level 1 Remember
CO 2	**Explain** various models for analysis of speech and audio signal	LOTS: Level 2 Understand
CO 3	**Apply** signal theory for the channel equalization, estimation	LOTS: Level 3 Apply
CO 4	**Analyze** various equalization and TDE techniques in signal processing.	HOTS: Level 4 Analyze
CO 5	**Design** various systems and identify various models for Speech, TDE, Equalization and DOA.	HOTS: Level 6 Create

UNIT-1

Speech and Audio Processing: Speech communication acoustic theory of speech: the source–filter model speech models and features. linear prediction models of speech harmonic plus noise model of speech fundamental frequency (pitch) information, speech coding, speech recognition, basic audio processing, hearing, psychoacoustics of hearing, speech analysis and classification, role of LPC coefficients in analysis filter. LPC stability issues.

UNIT-2

Time Delay Estimation: Need for the time delay estimation, system model, source localization strategies, ideal model-free field environment, TDE methods: cross-correlation function (CCF) method, least mean square (LMS) adaptive filter method, average square difference function (ASDF) method.

UNIT-3

Bayesian Inference and Channel Equalization:, Bayesian inference, basic definition, Bayesian theorem, elements of Bayesian inference, dynamics and probability model in estimation, parameter estimation and signal restoration, ML and MAP estimation, Introduction and need For Channel Equalization, Types of Equalization Techniques.

UNIT-4

System modeling and DOA: System identification based on FIR (MA), All Pole (AR), Pole Zero (ARMA) system models, Basic Principle of DOA Estimation, Need of DOA, Beamforming, Direction of Arrival, DOA Estimation Algorithms.

Reference Books:

1. Simon S Haykins, *"Adaptive Filter Theory"* Third Edition, PHI, 1996
2. John J. Proakis, *"Digital Signal Processing"* Second Edition, PHI, 1996
3. Andreas Antoniou, *"Digital Signal Processing"*, First Edition. Tata McGraw Hill, 2006.
4. DeFatta D J, Lucas J G and Hodgkiss W S, *"Digital Signal Processing"*, First Edition, J Wiley and Sons, 1988.
5. Walter, E., Pronzato, L, *"Identification of Parametric Models from Experimental Data"*, First Edition, Springer-Verlag, 1997.

Course Articulation Matrix:

Signal Processing (ECL-719)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	--	H	H	H
CO 2	H	--	H	H	H
CO 3	H	L	M	H	H
CO 4	H	L	H	H	H
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Digital VLSI Design Lab
ECP-716

General Course Information

Course Credits: 2 Contact Hours: 4/week (L-T-P: 0-0-4) Mode : Lab Work	**Course Assessment Methods (Internal: 50; External: 50)** The internal and external assessment is based on the level of participation in laboratory sessions, timely submission of experiments/assignments, the quality of solutions designed for the assignments, the performance in VIVA-VOCE, the quality of laboratory file and ethical practices followed. There will be a continuous process for laboratory course evaluation. Two internal examinations (each of 50 marks) for the laboratory courses (Minor Laboratory Evaluations: MLE I and MLE II) will be conducted in the week before or after the internal examinations for the theory courses. The overall internal marks will be calculated as the average of the two minor laboratory course evaluations. The course coordinator will conduct these minor evaluations in the slots assigned to them as per their timetable. The Chairperson of the Department will only notify the week for the internal laboratory course evaluations. The marks for MLE I and MLE II must be submitted within a week of the conduct of these laboratory course evaluations. The external examination will be conducted by external examiner appointed by the Controller of Examination along with the internal examiner, preferably the lab course coordinator, appointed by the Chairperson of the Department. The final practical examination of duration three hours will be conducted only in groups of 20-25 students. The Course Coordinator / Internal Examiners/ External Examiners will maintain and submit the bifurcation of marks obtained by the students in their respective internal/external evaluations in the specified proformas (attached herewith as Annexures I and II) to the respective departments in addition to the submitting and uploading of overall marks on the university portal as per the requirement of the result branch. The laboratory course coordinator will also conduct laboratory course exit survey and, compute and submit the attainment levels of the laboratory course based on direct and indirect evaluation components and submit it to the Chairperson office along with the internal assessment marks.

Pre-requisites: Digital Electronics, knowledge of various ICs

Course Objectives: This course aims at covering first the basic building block of the VLSI circuits, that is, start with MOSFET characteristics and then go through various logic circuits design using MOS transistors(like CMOS inverter, NAND NOR, MUX, DFF, Register) to complete Memory designs and layouts are also covered under this course.

Course Outcomes:

Sr. No.	At end of the semester, Student will be able to	RBT Level
CO 1	**Understand** software tools and apply these tools for the realisation of VLSI logic gates, circuits and systems.	LOTS: Levels 3 Apply
CO 2	**Compare** the outcomes of different experimental models.	HOTS: Level 4 Analyse
CO 3	**Evaluate** the performance of designed CMOS static & dynamic circuits and systems.	HOTS: Level 5 Evaluate
CO 4	**Integrate** knowledge of different CMOS circuits and systems for digital IC design.	HOTS: Level 6 Create
CO 5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO 6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

List of Experiments

1. To study the characteristics of MOS Device.
2. To design and simulate the CMOS Inverter Characteristics
3. To design and simulate the CMOS NAND gate
4. To design and simulate the CMOS NOR gate
5. To design and simulate the CMOS XOR gate
6. To design and simulate the CMOS Multiplexer
7. To design and simulate the CMOS SR Latch
8. To design and simulate the CMOS D-FF
9. To design and simulate the CMOS 1-bit Full Adder
10. To design and simulate the CMOS SRAM

Note: At least eight experiments are to be performed in the semester, out of which atleast six experiments should be performed from the given list. The remaining two experiments may either be performed from the list or designed & setup by the concerned institution as per the scope of the syllabus.

Course Articulation Matrix:

Digital VLSI Design Lab (ECP-716)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	M	H	H	H
CO 2	H	M	H	H	H
CO 3	H	M	H	H	H
CO 4	H	M	M	H	M
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Hardware Description Language Lab
ECP-717

General Course Information

Course Credits: 2 Contact Hours: 4/week (L-T-P: 0-0-4) Mode : Lab Work	**Course Assessment Methods (Internal: 50; External: 50)** The internal and external assessment is based on the level of participation in laboratory sessions, timely submission of experiments/assignments, the quality of solutions designed for the assignments, the performance in VIVA-VOCE, the quality of laboratory file and ethical practices followed. There will be a continuous process for laboratory course evaluation. Two internal examinations (each of 50 marks) for the laboratory courses (Minor Laboratory Evaluations: MLE I and MLE II) will be conducted in the week before or after the internal examinations for the theory courses. The overall internal marks will be calculated as the average of the two minor laboratory course evaluations. The course coordinator will conduct these minor evaluations in the slots assigned to them as per their timetable. The Chairperson of the Department will only notify the week for the internal laboratory course evaluations. The marks for MLE I and MLE II must be submitted within a week of the conduct of these laboratory course evaluations. The external examination will be conducted by external examiner appointed by the Controller of Examination along with the internal examiner, preferably the lab course coordinator, appointed by the Chairperson of the Department. The final practical examination of duration three hours will be conducted only in groups of 20-25 students. The Course Coordinator / Internal Examiners/ External Examiners will maintain and submit the bifurcation of marks obtained by the students in their respective internal/external evaluations in the specified proformas (attached herewith as Annexures I and II) to the respective departments in addition to the submitting and uploading of overall marks on the university portal as per the requirement of the result branch. The laboratory course coordinator will also conduct laboratory course exit survey and, compute and submit the attainment levels of the laboratory course based on direct and indirect evaluation components and submit it to the Chairperson office along with the internal assessment marks.

Pre-requisites: Digital Electronics

Course Objective: This course is for first year post graduation students. This course is designed to give students in hand practice of writing and simulating a Verilog code which is one of the popular hardware descriptive language. Various combinational and sequential circuits like simple logic gates, Half Adder, Full Adder, Multiplexer, Demultiplexer, Encoder, decoder, Flip-Flops, Shift Register, Counters are included.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO 1	**Understand** software tools and apply these tools for the modelling styles of Verilog HDL for logic, gates, circuits and systems design.	LOTS: Levels 3 Apply
CO 2	**Compare** the outcomes of different experimental models.	HOTS: Level 4 Analyse
CO 3	**Evaluate** the performance of logics design and verification of digital integrated circuits and systems.	HOTS: Level 5 Evaluate
CO 4	**Integrate** knowledge for design of digital circuits and systems for VLSI design, test and verification.	HOTS: Level 6 Create
CO 5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO 6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

List of Experiments

1. To design a Multiplexer Using Basic Gates in Verilog.
2. To design and describe a full adder in Verilog.
3. To design and describe an 8-bit ALU in Verilog.
4. To design and describe majority circuit in Verilog.
5. To design and describe latch and Flip-Flop in Verilog.
6. To design and describe D Type Flip-Flop with Synchronous and asynchronous Control in Verilog.
7. To design and describe a counter in Verilog.
8. To design and describe 8-bit universal shift register in Verilog.

9. To design and describe sequence detector in Verilog.

10. To implement any three design (given above) on FPGA kit.

Note: At least eight experiments are to be performed in the semester, out of which atleast six experiments should be performed from the given list. The remaining two experiments may either be performed from the list or designed & setup by the concerned institution as per the scope of the syllabus.

Course Articulation Matrix:

Hardware Description Language Lab (ECP-717)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	M	H	H	H
CO 2	H	M	H	H	H
CO 3	H	M	H	H	H
CO 4	H	M	M	H	M
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Embedded System Design Lab
ECP-718

General Course Information

Course Credits: 2 Contact Hours: 4/week (L-T-P: 0-0-4) Mode : Lab Work	**Course Assessment Methods (Internal: 50; External: 50)** The internal and external assessment is based on the level of participation in laboratory sessions, timely submission of experiments/assignments, the quality of solutions designed for the assignments, the performance in VIVA-VOCE, the quality of laboratory file and ethical practices followed. There will be a continuous process for laboratory course evaluation. Two internal examinations (each of 50 marks) for the laboratory courses (Minor Laboratory Evaluations: MLE I and MLE II) will be conducted in the week before or after the internal examinations for the theory courses. The overall internal marks will be calculated as the average of the two minor laboratory course evaluations. The course coordinator will conduct these minor evaluations in the slots assigned to them as per their timetable. The Chairperson of the Department will only notify the week for the internal laboratory course evaluations. The marks for MLE I and MLE II must be submitted within a week of the conduct of these laboratory course evaluations. The external examination will be conducted by external examiner appointed by the Controller of Examination along with the internal examiner, preferably the lab course coordinator, appointed by the Chairperson of the Department. The final practical examination of duration three hours will be conducted only in groups of 20-25 students. The Course Coordinator / Internal Examiners/ External Examiners will maintain and submit the bifurcation of marks obtained by the students in their respective internal/external evaluations in the specified proformas (attached herewith as Annexures I and II) to the respective departments in addition to the submitting and uploading of overall marks on the university portal as per the requirement of the result branch. The laboratory course coordinator will also conduct laboratory course exit survey and, compute and submit the attainment levels of the laboratory course based on direct and indirect evaluation components and submit it to the Chairperson office along with the internal assessment marks.

Pre-requisites: C languages & basic of digital and analog circuits

Course Objectives: The course is designed to provide hand-on experience to the students on the industry standard MP lab, KEIL make embedded Development boards related to PIC, ARM7 etc. processors. It provides students an opportunity to understand the architecture of latest micro- controllers through programming using KEIL software and development boards. The course familiarizes students with the interfacing of various application boards with development boards.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able:	RBT Level
CO 1	**Identify** software tools and apply these tools to write a program for microcontroller based applications.	LOTS: Level 1 Remember
CO 2	**Analyze** the outcomes of different experimental programs.	HOTS: Level 4 Analyse
CO 3	**Evaluate** the performance of different types of instructions set to write assembly language programs on different software.	HOTS: Level 5 Evaluate
CO 4	**Combine** knowledge for design of different types of microcontroller based applications through the use of timers & interrupts.	HOTS: Level 6 Create
CO 5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO 6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Appiy

List of Experiments

1. Write an assembly language program to perform addition & subtraction operation using PIC 16 Microcontrolier.
2. Write an assembly language program to perform multiplication and division operation using PIC 16 Microcontroller.
3. Write an assembly language program to perform logical operation using PIC 16 Microcontroller.
4. Write an assembly language progr m or d lay calculation using PIC Microcontroller.
5. Write a program for the blinking of LED's using PIC Microcontroller.

6. Familiarization with Keil software for 8051 & ARM based microcontroller programming.
7. To write and run 8051 assembly language program to perform MUL & DIV operations.
8. Write an asscmbly language program to add 16 bits using ARM.
9. Write an assembly language program for multiplying two 32 bit numbers using ARM.
10. Write an assembly language program to multiply two matrices using ARM.
11. Write an assembly language program for blinking an LED using Keil and display the result on ARM 7 microcontroller.
12. Write an assembly language program for LCD interfacing using CORTEX ARM microcontroller.

Note: At least eight experiments are to be performed in the semester, out of which atleast six experiments should be performed from the given list. The remaining two experiments may either be performed from the list or designed & setup by the concerned institution as per the scope of the syllabus.

Course Articulation Matrix:

Embedded System Design Lab (ECP-718)					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	H	L	M	H	H
CO 2	M	L	H	H	H
CO 3	H	M	H	H	H
CO 4	H	M	H	H	H
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

English For Research Paper Writing

AC01

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course objectives: This course is introduced to make students understand that how to improve your writing skills and level of readability and learn about what to write in each section. It also imparts the skills needed when writing a title and ensure the good quality of paper at very first-timesubmission.

Unit	Contents	Hours
1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	4
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
4	Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,	4
5	Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission	4

Reference books:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press Model Curriculum of Engineering & Technology PG Courses [Volume -II] [300].
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht HeidelbergLondon, 2011.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Disaster Management

AC02

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course Objective: - The course aims at the learning to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response. It makes students able to critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives. The course develops an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations. It also provides the ability to critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Units	Contents	Hours
1	**Introduction** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.	4
2	**Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Manmade disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	4
3	**Disaster Prone Areas In India** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics	4
4	**Disaster Preparedness And Management** Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.	4
5	**Risk Assessment** Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.	4
6	**Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	4

Reference books:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep & Deep Publication Pvt. Ltd., New Delhi.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Value Education

AC04

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course Objectives: This course makes students understand value of education and self-development. Imbibe good values in students Model Curriculum of Engineering & Technology PG Courses and let the students know about the importance of character.

Course outcomes: At the end of the course, students will be able to:

1. Gain knowledge of self-development.
2. Learn the importance of Human values.
3. Develop the overall personality.

Unit	Content	Hours
1	• Values and self-development –Social values and individual attitudes. • Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgments	4
2	• Importance of cultivation of values. • Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism. Love for nature ,Discipline	6
3	• Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. • Punctuality, Love and Kindness. • Avoid fault Thinking. • Free from anger, Dignity of labour. • Universal brotherhood and religious tolerance. • True friendship. • Happiness Vs suffering, love for truth. • Aware of self-destructive habits. • Association and Cooperation. • Doing best for saving nature	6
4	• Character and Competence –Holy books vs Blind faith. • Self-management and Good health. • Science of reincarnation. • Equality, Nonviolence, Humility, Role of Women. • All religions and same message. • Mind your Mind, Self-control. • Honesty, Studying effectively	6

Reference Book:

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press,New Delhi.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Stress Management By Yoga

AC07

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course Objectives: The course aims to achieve overall health of body and mind of the students and emphasizes upon overcoming the stress.

Course Outcomes: At the end of the course, students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also.
2. Improve efficiency.

Unit	Content	Hours
1	• Definitions of Eight parts of yog. (Ashtanga)	8
2	• Yam and Niyam. Do's and Don't's in life. i. Ahinsa, satya, astheya, bramhacharya and aparigraha ii. Shaucha, santosh, tapa, swadhyay, ishwarpranidhan	8
3	• Asan and Pranayam i. Various yog poses and their benefits for mind & body ii. Regularization of breathing techniques and its effects-Types ofpranayam	8

Reference books:

1. "Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal, Nagpur.
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata.

Second Semester

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Mobile Communication
ECL-721

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Communication System

Course Objectives: This course is introduced to develop basic understanding and impart in-depth knowledge of various concepts used in wireless mobile communication. The course imparts the concepts, parameters & models of mobile radio propagation also helps students understand the architecture and elements of wireless standards and systems like GSM, GPRS, CDMA, etc. It also provides coverage to the advanced, latest and upcoming wireless technologies like OFDM, Multicarrier Modulation, 4G, 5G, turbo codes and multi-user detection etc.

Course Outcomes:

Sr. No.	At end of the semester, students will be able to	RBT Level
CO 1	**Describe** terminologies & various generations of wireless communication systems and there technical specifications.	LOTS: Level 1 Remember
CO 2	**Explain** the concepts of cellular system, fading, multiple access techniques and multicarrier systems.	LOTS: Level 2 Understand
CO 3	**Apply** the concepts of radio planning for cellular mobile communication systems.	LOTS: Level 3 Apply
CO 4	**Evaluate** the performance of various wireless communication systems.	HOTS: Level 5 Evaluate
CO 5	**Design** basic wireless communication system in a better fashion with thorough knowledge of wireless communication technologies.	HOTS: Level 6 Create

UNIT-1

Introduction to Wireless Communication Systems: Various Generations of wireless mobile communication from 1G to 5G, The Cellular Concept, Frequency reuse, channel assignment strategies, hand-off strategies, interference and system capacity, improving capacity of cellular system through cell splitting, sectoring, etc.

UNIT-2

Mobile Radio Propagation: Introduction to radio wave propagation, three basic propagation mechanisms, Outdoor & indoor propagation models, small scale multipath propagation, parameters of mobile multipath channel, small scale & large scale fading, their types. **Wireless Systems:** Basic architecture of GSM, GPRS, 3G, 4G & 5G.

UNIT-3

CDMA System Concepts: Basics of CDMA. Spread spectrum concept. time hopping, Direct Sequence and Frequency Hopped Spread Spectrum, Chirp spread spectrum systems, Hybrid systems, Spreading sequences and their correlation functions, Code generation, Properties and generation of PN sequences, RAKE receiver, Diversity techniques an Rake receiver, Soft handoffs.

UNIT-4

Implementation Issues: OFDM, Multi-Carrier Modulation and Demodulation, Introduction to MIMO systems, Channel Coding and Decoding (Convolutional codes, Turbo codes), Multi-user Detection: Decorrelating detector, MMSE detector. Successive Interference Canceller, Parallel Interference Canceller.

Reference Books:

1. William, C Y Lee, "*Mobile Cellular Telecommunications*", Second Edition, McGraw Hill, 1995.
2. Kamilo Feher, "*Wireless and Digital Communications*" Second Edition, Prentice Hall, 1995.
3. G.L Stuber , "*Principles of Mobile Communication*", Fourth Edition, Springer, 2017.
4. T.S. Rappaport , "*Wireless Communication: Principles and Practice*", Second Edition, Pearson, 2014.
5. Raj Pandya, "*Mobile & Personal Communication Services & System*", First Edition, John Wiley, 2004.

Course Articulation Matrix:

Mobile Communication (ECL-721)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	--	H	H	M
CO 2	M	--	H	H	H
CO 3	H	L	H	M	H
CO 4	H	--	H	H	H
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Advance Optical Communication System
ECL-722

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Physics of optical communication components and applications to communication systems

Course Objectives: This course deals with the understanding of the optical components and the design and operation of optical fiber communication systems. The principles of wavelength division multiplexed (WDM) systems, SONET, SDH and passive optical networks. The characteristics and limitations of system components (laser diodes, external modulators, optical fiber, optical amplifiers, optical receivers) and the factors affecting the performance of the optical communication system.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Describe** the fundamentals and components of optical communication system.	LOTS: Level 1 Remember
CO 2	**Explain** the channel impairments, optical sources, detectors and non linearities etc. in optical communication system.	LOTS: Level 2 Understand
CO 3	**Apply** the fundamentals of optical communication for design of optical communication link as well as system.	LOTS: Level 3 Apply
CO 4	**Analyze** the performance of various optical communication systems.	HOTS: Level 4 Analyze
CO 5	**Design** optical fiber communication links using appropriate optical components.	HOTS: Level 6 Create

UNIT-1

Review: Evolution of Basic Fiber Optic Communication System, Benefits and disadvantages of Fiber Optics, Transmission Windows, Transmission Through Optical Fiber, The Numerical Aperture (NA), The Optical Fiber, Types of Fiber, Different Losses & Issues in Fiber Optics, Attenuation in Optical Fibers, Fiber Optic Loss Calculations, Dispersion, connectors & splices, bending loses, Absorption, scattering, very low loss materials, plastic & polymer-clad-silica fibers. Wave propagation in step index & graded index fiber, fiber dispersion, single mode fibers, multimode fibers, dispersion shifted fiber, dispersion flattened fiber, polarization, cut-off condition and V-parameter.

UNIT-2

Fiber Optic System Design Considerations and Components: Indoor Cables, Outdoor Cables, Cabling Example, Power Budget, Bandwidth and Rise Time Budgets, Electrical and Optical Bandwidth, Connectors, Fiber Optic Couplers.

Dispersion and Nonlinearities Dispersion in single mode and multimode fibers, dispersion shifted and dispersion flattened fibers, attenuation and dispersion limits in fibers, Kerr nonlinearity, self phase modulation, Cross Phase Modulation, FWM.

UNIT-3

Optical Sources: optical source properties, operating wavelength of optical sources, semiconductor light-emitting diodes and laser diodes, semiconductor material and device operating principles, light-emitting diodes, surface-emitting LEDS, edge-emitting LEDS, super luminescent diodes, laser diodes, comparison of LED and ILD. Fiber optic transmitters, basic optical transmitters, direct versus external modulation, fiber optic transmitter applications.

Optical Detectors: Basic Information on light detectors, Role of an optical detector, Detector

characteristics: Responsivity, Noise Equivalent Power, Detectivity, Quantum efficiency, The PN junction photo diode - PIN photodetectors - Avalanche photo diode construction characteristics and properties, APD Specifications, Applications of APD, Optical Receivers .

UNIT-4

Advanced Multiplexing Strategies: Optical TDM, subscriber multiplexing (SCM), WDM and Hybrid multiplexing methods.

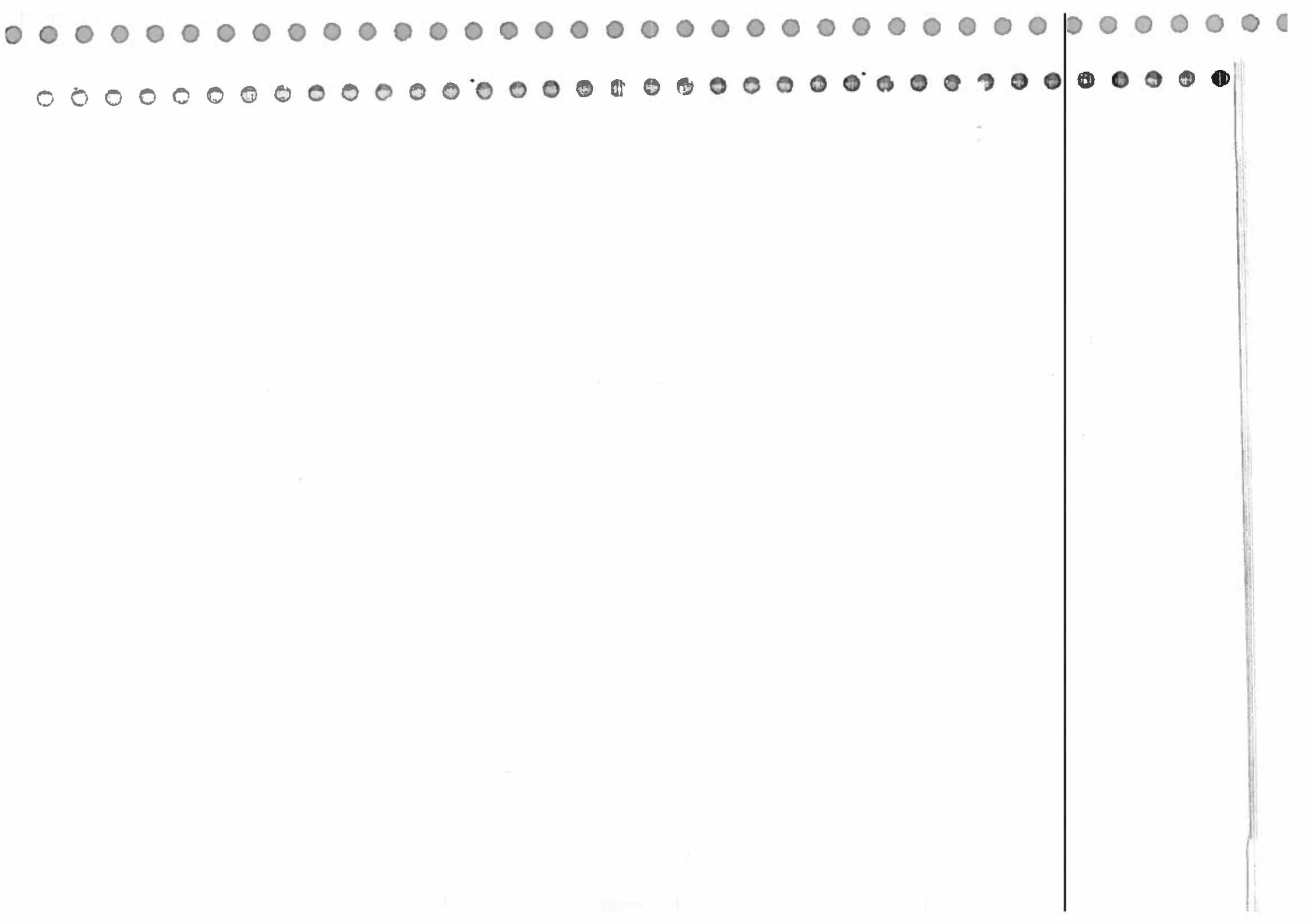
Optical Networking: Data communication networks, network topologies, MAC protocols, Network Architecture- SONET/TDH, optical transport network, optical access network, optical premise network.

Reference Books.

1. G.P Aggrawal, "*Fiber-Optic Communication Systems*", Fourth Edition, Wiley, 2010.
2. G. Keiser, "*Optical Fiber Communication*", Fifth Edition, Tata –McGraw Hill, 2013.
3. John Gowar, "*Optical communication Systems*", Second Edition, Prentice Hall, 1993.
4. John M. Senior, "*Optical Fiber Communications: Principles and Practice*", Third Edition, Pearson, 2014.
5. T L Singhal, "*Optical Fiber Communications*", First Edition, Cambridge University Press, 2016.

Course Articulation Matrix:

Advance Optical Communication System (ECL-722)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	--	M	H	M
CO 2	H	--	M	H	M
CO 3	H	--	M	H	M
CO 4	M	--	H	H	H
CO 5	M	--	H	H	H



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Analog IC Design
ECL-723

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Introduction to micro electronics circuits including bipolar and MOS transistors

Course Objectives: This Course is for the First year post-graduate students. The pre-requisite for the course is basic knowledge of semiconductor devices and an introduction to analog electronics. This course covers the design and analysis of various linear and non-linear analog circuits like amplifiers, current mirrors, comparators, oscillators, phase-locked loops etc. using both bipolar and MOS transistors various design parameters are covered.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO 1	**Describe** CMOS technologies for analog IC design.	LOTS: Level 1 Remember
CO 2	**Understand** analog CMOS circuits, systems and their uses.	LOTS: Level 2 Understand
CO 3	**Apply** the concepts of analog circuit design for the implementation of CMOS based integrated circuits and systems.	LOTS: Level 3 Apply
CO 4	**Analyze** large and small signal behaviour of analog circuits.	HOTS: Level 4 Analyze
CO 5	**Evaluate** large and small signal behaviour of analog circuits.	HOTS: Level 5 Evaluate
CO 6	**Design** analog CMOS circuits and systems.	HOTS: Level 6 Create

UNIT-1

Introduction to Analog Design, integrated circuits, CMOS Technology: brief history, levels of abstraction, robust analog design, basic MOS device physics-transistor and switch, MOS structure, MOSFET current voltage characteristics, second order effects, MOS models-small signal and large signal model, MOS capacitances, MOS SPICE model

UNIT- 2

Single stage amplifiers-common source, CS with resistive load, CS with diode connected load, CS with current source, CS triode load stage, CS with source degeneration, source follower, common gate, cascode stage, Differential amplifier, basic differential pair, common mode response, differential pair with MOS loads, DC transfer characteristics.

UNIT- 3

Basic MOS current mirrors, cascode current mirror, Wilson current mirror, widlar current mirror, voltage references, general considerations, supply independent biasing, temperature independent references, Operational Amplifier: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of one and two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS Folded-cascode operational amplifiers, Frequency response & compensation.

UNIT- 4

Nonlinear Analog Circuits: CMOS Comparators, Phase Locked Loops (PLL), closed loop analysis of PLL and applications. Voltage controlled oscillator, Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters, Operational transconductance Amplifier (OTA), Switched Capacitor circuits.

Reference Books:

1. Paul R. Gray, Paul J. Hurst, Stephen Lewis, and Robert G Meyer, *"Analysis and Design of Analog Integrated Circuits"*, Fifth Edition John Wiley & Sons, 2014.
2. Behzad Razavi, *"Design of Analog CMOS Integrated Circuits, Second Edition"*, McGraw Hill Education, 2014.
3. Randall L Geiger, *"VLSI Design Techniques for Analog and Digital Circuits"*, Second Edition, TMH, 1999.
4. Phillip E. Allen and Douglas R. Holberg, *"CMOS Analog Circuit Design"*, Second Edition, Oxford University Press, 2002.
5. D. A. Johns and Martin, *"Analog Integrated Circuit Design"*, Third Edition, John Wiley & Sons, 1997.
6. Behzad Razavi, *"Principles of data conversion system design"*, Second Edition, John Wiley & Sons, 2011.
7. R. Jacob Baker, *"CMOS-Circuit Design, Layout and Simulation"*, Third Edition, John Wiley & Sons, 2010.

Course Articulation Matrix:

Analog IC Design (ECL-723)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	L	H	H	H
CO 2	H	L	M	H	L
CO 3	M	L	H	H	M
CO 4	M	L	H	H	M
CO 5	M	L	H	H	M
CO 6	M	L	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Adaptive Signal Processing
ECL-724

General Course Information

Course Credits: 4 Type: Professional Core Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Signals and Systems, Digital Signal Processing

Course Objectives: To introduce the concepts and techniques associated with the understanding of digital signal processing. To familiarize with techniques suitable for analyzing and synthesizing both continuous-time and discrete time systems. To provide with an appreciation of applications for the techniques and mathematics used in this course.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Describe** the significance of signal processing in the fields of computing and telecommunications.	LOTS: Level 1 Remember
CO 2	**Explain** various digital filters used in signal processing.	LOTS: Level 2 Understand
CO 3	**Apply** adaptive algorithm for the analysis of adaptive filtering application	LOTS: Level 3 Apply
CO 4	**Evaluate** various models for adaptive filtering application	HOTS: Level 5 Evaluate
CO 5	**Design** various types of filter used in signal processing.	HOTS: Level 6 Create

UNIT-1

Basic of Digital Signal Processing: Signals and Information, Signal Processing Methods, Applications of Digital Signal Processing, Derivation of the z-Transform Properties of z-Transform, Fourier series and Fourier transform. Random variable, Stochastic processes.

UNIT-2

Design of Digital Filters: Introduction, Linear Time-Invariant Digital Filters, Recursive and Non-Recursive Filters, Filtering Operation, Sum of Vector Products, A Comparison of Convolution and Correlation, Filter Structures, Direct, Cascade and Parallel Forms, Linear Phase FIR Filters Design of Digital FIR Filter-banks, Sub-band Filters, Design of Infinite Impulse Response IIR filters, Issues in the Design and Implementation of a Digital Filter.

UNIT-3

Adaptive Filtering: introduction to random process, Basic of adaptive filtering. Performance function, factors determining the choice of algorithm, method of Steepest-Descent, LMS algorithm, modified LMS algorithm, Normalized LMS algorithm, important properties of LMS, implementation consideration, Computational issues.

UNIT-4

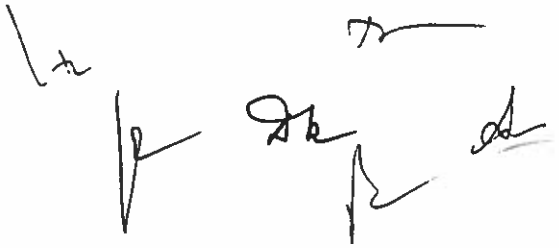
Adaptive Filter Applications: Adaptive echo cancellation, Principle of adaptive echo cancellation, Sub band acoustic echo cancellation, echo cancellation with linear prediction pre whitening, Stereophonic echo cancellation Performance evaluation of echo canceller, Adaptive noise cancellation, Adaptive line enhancer.

Reference Books:

1. Simon S Haykins, *"Adaptive Filter Theory"*, Third Edition, PHI, 1996
2. John J. Proakis, *"Digital Signal Processing"*, Second Edition, PHI, 1997.
3. Harry L. Van Trees, *"Detection, Estimation, and Modulation Theory, Part 1&3,"*, First Edition, Wiley. 2002.
4. Saeed V. Vaseghi, *"Advanced Digital Signal Processing and Noise Reduction,"* Third Edition, PHI, 2006.
5. Eberhard Hänsler, *"Gerhard Schmidt Acoustic Echo and Noise Control: A Practical Approach,"* Wiley, 2005.

Course Articulation Matrix:

Adaptive Signal Processing (ECL-724)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	--	--	M	H	M
CO 2	L	L	H	M	H
CO 3	L	--	M	H	H
CO 4	M	L	M	H	H
CO 5	M	L	H	H	H



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Algorithm for VLSI Design Automation

ECL-725(i)

General Course Information

Course Credits: 4 Type: Program Elective Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: VLSI Design

Course Objectives: This course is for first year post graduation students. This course is designed to demonstrate the use of data structure to build up the CAD tools for simulation, synthesis and physical VLSI design.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able:	RBT Level
CO 1	**Define & describe** the terminology and fundamental principles related to VLSI design automation.	LOTS: Level 1 Remember
CO 2	**Understand & expiain** logic synthesis, VLSI automation algorithms, routing algorithms, VLSI compaction.	LOTS: Level 2 Understand
CO 3	**Apply** the various VLSI automation algorithms for high-level synthesis.	LOTS: Level 3 Apply
CO 4	**Analyze** the significance of VLSI automation algorithms, routing algorithms, via minimization and VLSI compaction.	HOTS: Level 4 Analyze
CO 5	**Design & develop** hardware models for VLSI design based applications.	HOTS: Level 6 Create

UNIT-1

Logic synthesis & verification: Introduction to combination all logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT-2

VLSI automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint-based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

UNIT-3

Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switch box routing algorithms.

UNIT-4

Over the cell routing & via minimization: two layers over the cell routers, constrained &unconstrained via minimization.

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction.

Reference Books:

1. Naveed Shervani, *"Algorithms for VLSI physical design Automation"*, Second Edition Kluwer Academic Publisher, 2002.
2. Christophn Meinel & Thorsten Theobold, *"Algorithm and Data Structures for VLSI Design"*, First Edition, KAP, 2002.

3. Rolf Drechsheler, *"Evolutionary Algorithm for VLSI"*, Second Edition, Kluwer Academic Publisher, 2002.
4. Trimburger, *"Introduction to CAD for VLSI"*, First Edition, Kluwer Academic Publisher, 2002.
5. Parhami, B., *"Computer Arithmetic: Algorithms and Hardware Design"*, First Edition, Oxford University Press, 2000.
6. Pinaki Mazumder, E. Mrudnick, *"Genetic Algorithm for VLSI Design, Layout and Test Automation"*, First Edition, Prentice Hall, 1998.

Course Articulation Matrix:

Algorithm for VLSI Design Automation (ECL-725(i))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	--	H	H	M
CO 2	H	--	H	H	M
CO 3	H	L	H	H	H
CO 4	H	L	H	H	H
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Advanced Computer Architectures
ECL-725(ii)

General Course Information

Course Credits: 4 Type: Program Elective Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Basics of digital electronics and computer organization

Course Objectives: Understand the architecture of a modern computer with its various processing units and the performance measurement of the computer system. The course also provides knowledge about memory management system of computer.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Define** the terminology and fundamental principles related to advanced computer architectures.	LOTS: Level 1 Remember
CO 2	**Explain** parallel computer models, advanced/multiprocessor architecture, memory, designs/architecture.	LOTS: Level 2 Understand
CO 3	**Demonstrate** computer models and architecture, network properties, memory organizations and architecture.	LOTS: Level 3 Apply
CO 4	**Analyze** the significance of pipelining, interconnections, memory hierarchy organizations and protocols.	HOTS: Level 4 Analyze

UNIT-1

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.
Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

UNIT-2

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems. Crossbar switch and multiport memory, Multistage and combining network.
Advanced processors: Advanced processor technology, Instruction- set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors Pipelining: Linear pipeline processor, non linear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multi functional arithmetic pipelines.

UNIT-3

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multi level cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenge of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization.

UNIT-4

Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.

Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine check, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.

Reference Books

1. Kai Hwang, "*Advanced computer architecture: Parallelism, Scalability and Programmability*"; First edition, TMH, 2003.
2. D.A.Patterson and John L hennessey, "*Computer organization and Design*", Elseveir, Fifth Edition, 2014.
3. Kai Hwang, "*Advanced Computer architecture Parallelism, scalability ,Programmability*", First Edition, Mc Graw Hill, 2003.
4. Kai Hwang and F.A.Briggs, "*Computer Architecture and Parallel Processor*" First Edition, Mc Graw Hill, 1999.
5. Shaungbao Paul Wang, "*Computer Architecture and Organization: Fundamentals and Architecture Security*", First Edition, Springer, 2021.
6. J. L. Hennessy, and D.A. Patterson, "*Computer Architecture: A quantitative approach*", Fifth Edition, Morgan Kaufman Publication, 2012

Course Articulation Matrix:

Advanced Computer Architectures (ECL-725(ii))					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	M	--	H	H	M
CO 2	M	--	H	H	H
CO 3	H	L	M	H	H
CO 4	H	L	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MEMS & IC Integration

ECL-725 (iii)

General Course Information

Course Credits: 4 Type: Program Elective Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: IC fabrication techniques, Analog & Digital VLSI design.

Course Objectives: This course has been developed due to industry request and as an introduction to a growing and important field in our high technology future. The objectives of this course are to teach critical thinking in micro engineering process, materials and design issues, to build an understanding of micro scale physics for use in designing MEMS applications, review current MEMS, RFMEMS and Bio MEMS applications, use the above knowledge to design and fabricate novel EMS/Bio MEMS /RF MEMS applications as part of a group project.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Describe** the terminologies used in MEMS & IC fabrication.	LOTS: Level 1 Remember
CO 2	**Explain** basic approach to various micro-sensors, micro-actuators, their types and applications.	LOTS: Level 2 Understand
CO 3	**Apply** their understanding in fabrication process and characterization of MEMS & ICs.	LOTS: Level 3 Apply
CO 4	**Summarize** the performance of MEMS devices and ICs based on their characterization results.	HOTS: Level 5 Evaluate
CO 5	**Compile** various simple micro-devices and micro-systems.	HOTS: Level 6 Create

UNIT-1

MEMS Fabrication: Conventional MEMS fabrication using VLSI technology: lithography, chemical etching: isotropic and anisotropic, Plasma etching, Reactive ion etching, Oxidation, Chemical vapor deposition, LPCVD, PECVD, Surface micromachining, LIGA, single layer and higher layer fabrication, Non-conventional MEMS fabrication: laser micromachining and welding micromachining(EDM & ECM), dynamic mask process, Electronic packaging.

UNIT-2

MEMS Sensors: Physical Micro Sensors: Classification of physical sensors, Integrated, Intelligent, or Smart Sensors. Sensing mechanisms: Piezoresistive sensing, Capacitive sensing, Piezoelctric sensing, Resonant sensing. Inter digital Transducer (IDT) and Surface Acoustic Waves (SAW) sensor. Microactuation: Electrostatic Actuation, Magnetic Actuation, Piezoelectric Actuation, Thermal Actuation.

UNIT-3

MEMS Design & Analysis: Basic concepts of design of MEMS devices and processes, Design for fabrication, Other design considerations, Analysis of MEMS devices, Modeling and Simulation.

UNIT-4

MEMS Characterization: Technologies for MEMS characterization, Scanning Probe Microscopy (SPM), Atomic Force Microscopy (AFM), Scanning Tunneling Microscopy (STM), Magnetic Force Microscopy, Scanning Electron Microscope.

Reference Books:

1. G. T. A. Kovacs, *"Micro machined Transducers Source book"*, First Edition, The McGraw-Hill, Inc. 1998
2. S. D. Senturia, *"Microsystem Design"*, First Edition, Kluar Publishers, 2001
3. N. Maluf and K. Williams, *"An Introduction to Microelectromechanical Systems Engineering"*, Second Edition, Artech House, 2004.
4. M. Tabib-Azar, *"Microactuators: Electrical, Magnetic, Thermal, Optical, Mechanical, Chemical and Smart Structures"*, First Edition, Kluwer Academic Publishers, 1998.
5. H. J. Santos, *"Introduction to Microelectromechanical (MEM) Microwave Systems"*, First Edition, Artech House Publishers, 1999.

Course Articulation Matrix:

MEMS & IC Integration (ECL-725 (iii))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	L	H	H	H
CO 2	H	L	H	H	H
CO 3	H	--	H	H	H
CO 4	H	L	H	H	H
CO 5	H	--	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Organic Semiconductors
ECL-725 (iv)

General Course Information

Course Credits: 4 Type: Program Elective Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Pre-requisites: Analog and digital electronics, Semiconductors

Course Objectives: This is the very first course for the post-graduate students. This course first provides the foundation of for the organic electronics. It provides the basic details like structure of organic semiconductors, charge transport in organic semiconductors, structure of diffe.. de.ices like OLEDs, OPVs and OFETs. After taking this course, the student should be able to demonstrate theoretical knowledge on the concept of organic semiconductors and working of organic devices like OLED, OPV and OFET.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Describe** basic terminology related to organic semiconductors.	LOTS: Level 1 Remember
CO 2	**Explain** various optical and electrical properties of organic semiconductors.	LOTS: Level 2 Understand
CO 3	**Demonstrate** knowledge of electrical properties in organic semiconductor devices.	LOTS: Level 3 Apply
CO 4	**Differentiate** various organic semiconducting devices used in the industry.	HOTS: Level 4 Analyze
CO 5	**Summarize** different organic semiconducting device like OLED, OFET & OPVs.	HOTS: Level 5 Evaluate

UNIT-1

Introduction to Organic Semiconductors: Concept of organic semiconductors, Electronic & molecular orbitals, carrier density in intrinsic semiconductors.

Charge transport in organic semiconductors: Charge transport via Hopping Mechanism, Doping in organic semiconductors, Charge transport in disordered semiconductors.

UNIT-2

Characterization: Microstructural Characterization of Organic Semiconductors using XRD, Use of SEM for crystal size calculation, Optical Characterization using PL and UV-Vis spectroscopy, Electrical characterization.

UNIT-3

Device application of Organic Semiconductors: Device structure and working of OFETS, OPVs and OLEDs.
Device fabrication techniques: Physical Vapor deposition, Chemical vapor deposition, Spin coating, Sputtering.

UNIT-4

Advanced Organic devices and Sensors: Organic sensors in medical, organic sensors in mechanical applications, sensing mechanism basics.

References Books:

1. J. E. Morris and K. Iniewski, *"Nanoelectronic Device Applications Handbook"*, First Edition, CRC Press, 2017.
2. L. R. Dalton and S. Sun, *"Introduction to Organic Electronic and Optoelectronic Materials and Devices"*, Second Edition, CRC Press, 2019.
3. S. Ogawa, *"Organic Electronics Materials and Devices"*, First Edition, Springer, 2016.
4. P. Cosseddu, M. Caironi, *"Organic Flexible Electronics Fundamentals Devices and Applications"*, First Edition, Elsevier Science, 2020.
5. Hari Singh Nalwa, *"Handbook of Organic Electronics and Photonics"*, American Scientific Publishers, Second Volume, 2008.

Course Articulation Matrix:

Organic Semiconductors (ECL-725 (iv))					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	L	--	M	H	M
CO 2	H	--	M	H	H
CO 3	L	L	H	H	H
CO 4	L	--	M	H	H
CO 5	H	--	H	M	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Artificial Intelligence
ECL-725 (v)

General Course Information

Course Credits: 4 Type: Elective Contact Hours: 4 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: ProbabilityTheory, Mathematics.

Course Outcomes:

Sr.No.	At the end of the semester, students will be able to:	RBT Level
CO1	**Outline & recall** the terminology, general architecture and application areas for artificial intelligence and machine learning.	LOTS: Level 1 Remember
CO2	**Understand** the various artificial intelligence and machine learning algorithms.	LOTS: Level 2 Understand
CO3	**Apply** the knowledge gained to solve given problem.	LOTS: Level 3 Apply
CO4	**Analyze & evaluate** the performance of various artificial intelligence and machine learning algorithms.	HOTS: Level 4 & 5 Analyze & Evaluate

Course Content

UNIT-1

Introduction: Introduction to Artificial Intelligence, Applications of Artificial Intelligence, Intelligent Agents, Structure of Intelligent Agents.

Introduction to Search: Searching for solutions, Uninformed search strategies, Informed Search Strategies, Local search algorithms and optimistic problems, Adversarial Search, Search for games, Alpha-beta pruning.

UNIT-2

Knowledge Representation & Reasoning: Propositional logic, First order Logic, Inference in propositional logic and First order logic.Fuzzy Logic: Basic concepts of Fuzzy logic, Fuzzy vs Crisp set, Linguistic variables, membership functions, operations of Fuzzy sets, Fuzzy if thenrules.Fuzzy relations, Operations on fuzzy relations, defuzzificationtechniques.

UNIT-3

Machine Learning: Supervised, unsupervised and reinforcement learning, Pattern recognition: Introduction and Design principles.Supervised Learning: Introduction to linear regression, estimating the coefficients, Accessing the accuracy of the regression model, basic decision tree learning (ID3) algorithm, k-nearest neighbour learning.Unsupervised Learning: About clustering, type of data in clustering analysis, k-means and k-medoids, Performance analysis of clustering algorithms.

UNIT-4

Deep Learning: Artificial neural network: introduction, learning rules, perceptron network, Back Propagation Neural Networks: Architecture, Gradient descent learning rule, Convolutional Neural Network: Architecture, Convolutional layer, Activation layer, Pooling layer, flatten layer, fully connected layer, dropout layer.

Text Books:

1. Stuart Russell, Peter Norvig, *"Artificial Intelligence- A Modern Approcah"*, Pearson Education.
2. S.N. Sivanandam, S. Sumathi, S.N. Deepa, *"Introduction to Neural Networks using MATLAB 6.0"*, McGraw Hill Education.
3. S. Rajasekaran & G.A.Vijayalakshmi Pai, *"Neural Networks, Fuzzy Logic and Genetic Algorithms: Synthesis & Applications"*,PHI.
4. Aurelien Geron, " *Hands on Machine Learning with Scikit-Learn & TensorFlow"*, O'Reilly Media Inc.
5. Elaine Rich, Kevin Knight and Shivashankar B Nair, *"Artificial intelligence"*, McGraw Hill Education.

6. B.Yegnanarayana, *"Artificial Neural Networks"*, Prentice Hall of India.
7. Satish Kumar, *"Neural Networks – A Classroom Approach"*, Tata McGraw-Hill.
8. S.Haykin, *"Neural Networks – A Comprehensive Foundation"*, Prentice Hall.

Course Articulation Matrix:

Artificial Intelligence (ECL-725 (v))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	-	-	L	L	L
CO 2	L	-	M	L	L
CO 3	L	-	M	M	M
CO 4	M	-	M	M	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Adaptive Signal Processing Lab
ECP-726

General Course Information

Course Credits: 2 Contact Hours: 4/week (L-T-P: 0-0-4) Mode : Lab Work	**Course Assessment Methods (Internal: 50; External: 50)** The internal and external assessment is based on the level of participation in laboratory sessions, timely submission of experiments/assignments, the quality of solutions designed for the assignments, the performance in VIVA-VOCE, the quality of laboratory file and ethical practices followed. There will be a continuous process for laboratory course evaluation. Two internal examinations (each of 50 marks) for the laboratory courses (Minor Laboratory Evaluations: MLE I and MLE II) will be conducted in the week before or after the internal examinations for the theory courses. The overall internal marks will be calculated as the average of the two minor laboratory course evaluations. The course coordinator will conduct these minor evaluations in the slots assigned to them as per their timetable. The Chairperson of the Department will only notify the week for the internal laboratory course evaluations. The marks for MLE I and MLE II must be submitted within a week of the conduct of these laboratory course evaluations. The external examination will be conducted by external examiner appointed by the Controller of Examination along with the internal examiner, preferably the lab course coordinator, appointed by the Chairperson of the Department. The final practical examination of duration three hours will be conducted only in groups of 20-25 students. The Course Coordinator / Internal Examiners/ External Examiners will maintain and submit the bifurcation of marks obtained by the students in their respective internal/external evaluations in the specified proformas (attached herewith as Annexures I and II) to the respective departments in addition to the submitting and uploading of overall marks on the university portal as per the requirement of the result branch. The laboratory course coordinator will also conduct laboratory course exit survey and, compute and submit the attainment levels of the laboratory course based on direct and indirect evaluation components and submit it to the Chairperson office along with the internal assessment marks.

Pre-requisites: Basic of MATLAB, Concept of digital signal processing and adaptive digital signal processing.

Course Objectives: This course is designed to demonstrate the use of MATLAB and other open source software for simulation, synthesis and designing of different processing systems. Apart from this working with the DSP processor hardware is familiarized.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Show** software tools and apply these tools for the realization of various filter designs.	LOTS: Levels 3 Apply
CO 2	**Compare** the outcomes of different experimental models.	HOTS: Level 4 Analyze
CO 3	**Evaluate** the performance of different windowing techniques to design various filters.	HOTS: Level 5 Evaluate
CO 4	**Integrate** knowledge for design of various tools and commands for interference cancellation and direction of arrival	HOTS: Level 6 Create
CO 5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO 6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

List of Experiments

1. To write Matlab statement for Algebraic Equations.
2. To write a program for adaptive filter application in interference cancellation.
3. To write a program for Direction of arrival estimation.
4. To write a program for filter design with the help of Matlab filter design tool.
5. To write a program for designing filters from Windowing techniques.
6. To write a program for to find the Power spectral Density.
7. To simulate the given model using simulink tool.
8. To write a program for cross correlation and auto correlation.
9. To familiarize with working of DSP Processor & Hardware.

Note: At least eight experiments are to be performed in the semester, out of which atleast six experiments should be performed from the given list. The remaining two experiments may either be performed from the list or designed & setup by the concerned institution as per the scope of the syllabus.

Course Articulation Matrix:

Adaptive Signal Processing Lab (ECP-726)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	M	M	H	H
CO 2	M	L	M	H	H
CO 3	H	M	M	H	H
CO 4	M	L	M	H	H
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Sanskrit For Technical Knowledge

AC03

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course Objectives: The course is aimed To get a working knowledge in illustrious Sanskrit, the scientific language in the world as Learning of Sanskrit to improve brain functioning. It helps to develop the logic in mathematics, science & other subjects enhancing the memory power. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from the ancient literature.

Course Outcomes: Students will be able to

1. Understanding basic Sanskrit language.
2. Ancient Sanskrit literature about science & technology can be understood.
3. Being a logical language will help to develop logic in students.

Unit	Content	Hours
1	• Alphabets in Sanskrit, • Past/Present/Future Tense, • Simple Sentences	8
2	• Order • Introduction of roots • Technical information about Sanskrit Literature	8
3	• Technical concepts of Engineering-Electrical, Mechanical, Architecture,Mathematics	8

Reference Books:

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi.
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam,New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

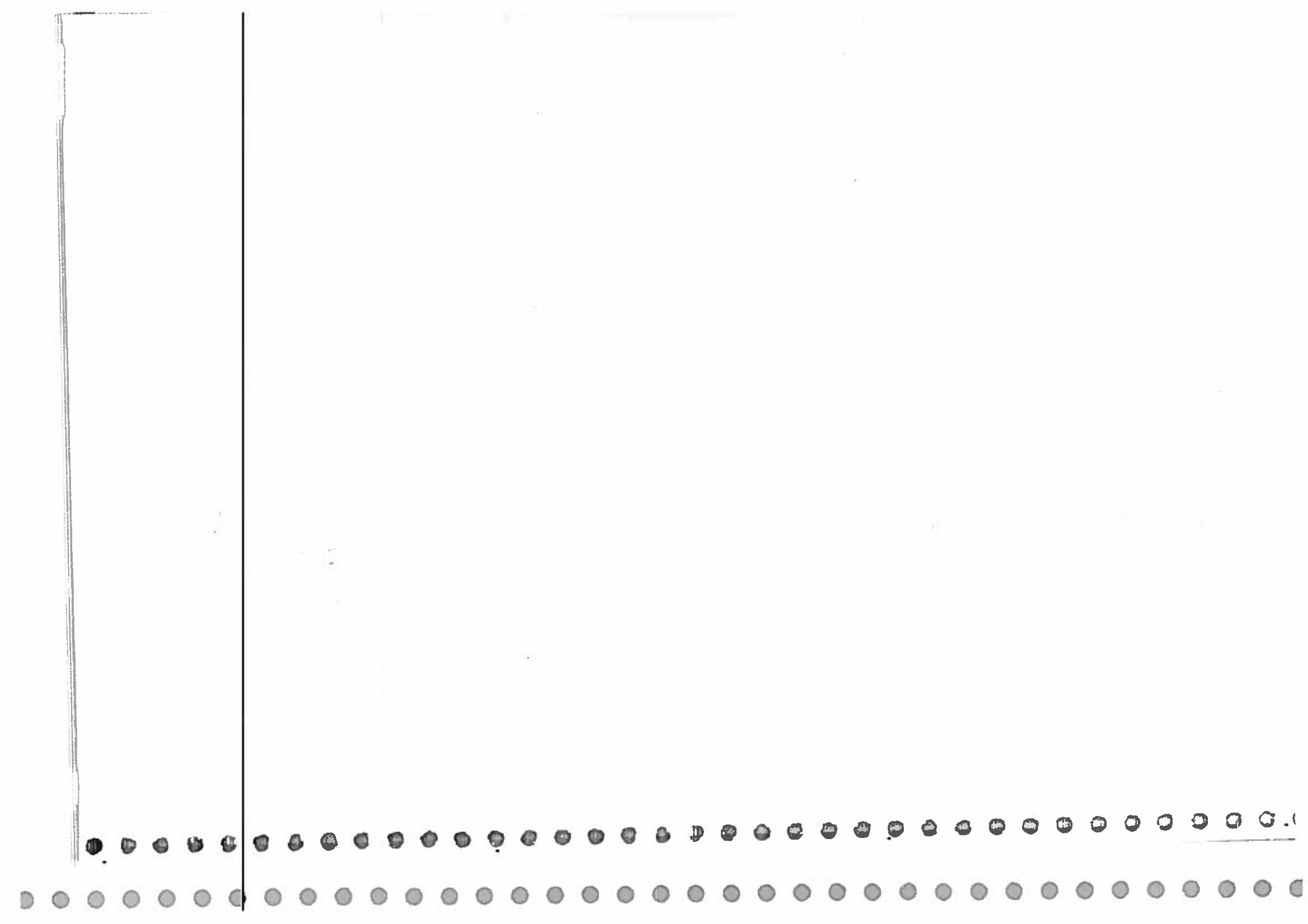
Constitution of India

AC05

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course Objectives: The course is introduced to make students understand the premises informing the twin themes of liberty and freedom from a civil rights perspective. It helps to address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism. The course also addresses the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.



Course Outcomes: Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival ofGandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of socialreforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adultsuffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

Units	Content	Hours
1	• **History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	• **Philosophy of the Indian Constitution:** Preamble Salient Features	4
3	• **Contours of Constitutional Rights & Duties:** ▪ Fundamental Rights ▪ Right to Equality ▪ Right to Freedom ▪ Right against Exploitation ▪ Right to Freedom of Religion ▪ Cultural and Educational Rights ▪ Right to Constitutional Remedies ▪ Directive Principles of State Policy ▪ Fundamental Duties.	4
4	• **Organs of Governance:** ▪ Parliament ▪ Composition ▪ Qualifications and Disqualifications ▪ Powers and Functions ▪ Executive ▪ President ▪ Governor ▪ Council of Ministers ▪ Judiciary, Appointment and Transfer of Judges, Qualifications ▪ Powers and Functions	4
5	• **Local Administration:** ▪ District's Administration head: Role and Importance,	4
	▪ Municipalities: Introduction, Mayor and role of Elected representative, CEO of Municipal Corporation. ▪ Pachayati raj: Introduction, PRI: Zila Pachayat. ▪ Elected officials and their roles, CEO Zila Pachayat: Position and role. ▪ Block level: Organizational Hierarchy (Different departments), ▪ Village level: Role of Elected and Appointed officials, ▪ Importance of grass root democracy	

6	• **Election Commission:** ▪ Election Commission: Role and Functioning. ▪ Chief Election Commissioner and Election Commissioners. ▪ State Election Commission: Role and Functioning. ▪ Institute and Bodies for the welfare of SC/ST/OBC and women.	4

Reference Books:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Pedagogy Studies

AC06

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course Objectives: The course helps students to review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers. It also helps to identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developingcountries?
2. Model Curriculum of Engineering & Technology PG Courses [Volume -II] [306]
3. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with whatpopulation of learners?

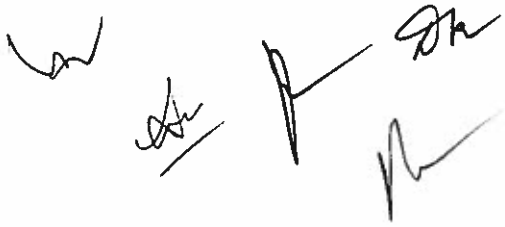
4. How can teacher education (curriculum and practicum) and the school curriculum and guidance materialsbest support effective pedagogy?

Units	Content	Hours
1	• **Introduction and Methodology:** ▪ Aims and rationale, Policy background, Conceptual framework and terminology ▪ Theories of learning, Curriculum, Teacher education. ▪ Conceptual framework, Research questions. ▪ Overview of methodology and Searching.	4
2	▪ Thematic overview: Pedagogical practices are being used by teachers in formaland informal classrooms in developing countries. ▪ Curriculum, Teacher education.	2
3	▪ Evidence on the effectiveness of pedagogical practices ▪ Methodology for the in depth stage: quality assessment of included studies. ▪ How can teacher education (curriculum and practicum) and the schoolcurriculum and guidance materials best support effective pedagogy? ▪ Theory of change. ▪ Strength and nature of the body of evidence for effective pedagogical practices. ▪ Pedagogic theory and pedagogical approaches. ▪ Teachers' attitudes and beliefs and Pedagogic strategies.	4
4	▪ Professional development: alignment with classroom practices and follow-upsupport ▪ Peer support ▪ Support from the head teacher and the community. ▪ Curriculum and assessment ▪ Barriers to learning: limited resources and large class sizes	4
5	• **Research gaps and future directions** ▪ Research design ▪ Contexts ▪ Pedagogy ▪ Teacher education ▪ Curriculum and assessment ▪ Dissemination and research impact.	2

Reference Books:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning

of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational development, 33(3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Personality Development Through Life Enlightenment Skills

AC08

General Course Information

Course Credits: 0 Type: Audit Course Contact Hours: 2 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods (internal: 30; external: 70) Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks.

Course Objectives: This course helps students to learn to achieve the highest goal happily. To become a person with stable mind, pleasing personality and determination. To awaken wisdom in students

Course Outcomes: Students will be able to:

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve thehighest goal in life.
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity.
3. Study of Neetishatakam will help in developing versatile personality of students.

Unit	Content	Hours
1	Neetisatakam-Holistic development of personality • Verses- 19,20,21,22 (wisdom) • Verses- 29,31,32 (pride & heroism) • Verses- 26,28,63,65 (virtue) • Verses- 52,53,59 (dont's) • Verses- 71,73,75,78 (do's)	8
2	• Approach to day to day work and duties. • Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48, • Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, • Chapter 18-Verses 45, 46, 48.	8
3	• Statements of basic knowledge. • Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 • Chapter 12 -Verses 13, 14, 15, 16,17, 18 • Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17,Chapter 3-Verses 36,37,42, • Chapter 4-Verses 18, 38,39 • Chapter18 – Verses 37,38,63	8

Reference Books:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

Third Semester

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINNERING

Mixed-Signal Design

ECL-731 (i)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Digital System Design, Analog IC Design

Course Objectives: The course provides an overview of Mixed Signal CMOS VLSI Design, particularly signals, data converters and deals with both the function of related components and system performance. The classification of various filters, data converts with practical implementation are demonstrated using characterizing parameters.

Course Outcomes:

Sr. No.	At the end of the semester, Student will be able to	RBT Level
CO 1	**Describe** CMOS analog and digital mixed signal circuits and systems and their technical specifications and uses.	LOTS: Level 1 Remember
CO 2	**Understand** various CMOS analog and digital mixed signal circuits and systems topologies.	LOTS: Level 2 Understand
CO 3	**Apply** the concepts of CMOS analog and digital mixed signal logics for the design of integrated circuits and systems.	LOTS: Level 3 Apply
CO 4	**Analyze** CMOS analog and digital mixed signal circuits and systems.	HOTS: Level 4 Analyze
CO 5	**Evaluate** CMOS analog and digital mixed signal circuits and systems.	HOTS: Level 5 Evaluate
CO 6	**Design** CMOS analog and digital mixed signal circuits and systems for IC design, test and verification.	HOTS: Level 6 Create

Course Contents

UNIT-1

Signals, Filters and Tools-Sinusoidal Signals, Comb Filters. Representing Signals, Exponential Fourier Series, Fourier Transform, Dirac Delta Function, Sampling and Aliasing: Sampling and circuits- Impulse Sampling, The Sample-and-Hold (S/H), S/H Spectral Response and implementation, The Reconstruction Filter, The Track-and-Hold (T/H), Interpolation, Zero Padding, Hold Register, Linear Interpolation, K-Path Sampling, Switched-Capacitor Circuits, Non-Overlapping Clock Generation

UNIT-2

Analog Filters: Integrator Building Blocks: Lowpass Filters, Active-RC Integrators, MOSFET IC Integrators, gm-C (Transconductor-C) Integrators, Common-Mode Feedback Considerations, Discrete-Time Integrators, Exact Frequency Response of an Ideal Discrete-Time Filter, Filtering Topologies: The Bilinear Transfer Function, The Biquadratic Transfer Function, High Q, Q Peaking and Instability

Digital Filters: SPICE Models for DACs and ADCs, The Ideal DAC and AD, Sinc-Shaped Digital Filters, LowpassSinc Filters, Filtering topologies, The Biquadratic Transfer Function, Comparing Biquads to Sinc-Shaped Filters

UNIT-3

Data Converter SNR- Quantization Noise, Quantization Noise Voltage Spectral Density, Calculating Quantization Noise from a SPICE Spectrum, Power Spectral Density, Signal-to-Noise Ratio (SNR): Effective Number of Bits, Coherent Sampling, Signal-to-Noise Plus Distortion Ratio, Spurious Free Dynamic Range, Dynamic Range, Specifying SNR and SNDR, Clock Jitter, Using Oversampling to Reduce Sampling Clock Jitter, Stability Requirements, Improving SNR using Averaging, Ideal Signal-to-Noise Ratio, Linearity requirements. Data Converter Design Basics: The One-Bit ADC and DAC, Improving SNR and Linearity, Revisiting Switched Capacitor Implementations, Improving Linearity Using an Active Circuit.

UNIT-4

Noise-Shaping Data Converters: First-Order Noise Shaping, Second-Order Noise-Shaping, Noise-Shaping Topologies, Bandpass Data Converters: Continuous-Time Bandpass Noise Shaping, Active-Component Bandpass Modulators, Switched-Capacitor Bandpass Noise Shaping, A High-Speed Data Converter: The Topology, Clock Signals, Path Settling Time, Implementation, Filtering, Practical Implementation

Reference Book:

1. R. J. Baker, *"CMOS Mixed Signal Circuit Design"*, Second Edition, John Wiley& Sons, 2011.
2. Handkiewicz, *"Mixed-Signal Systems: A Guide to CMOS Circuit Design"*, First Edition, John Wiley & Sons, 2015.
3. P. V. A. Mohan, V. Ramachandran and M. N. S. Swamy, *"Switched CapacitorFilters: Theory, Analysis and Design"*, Third Edition, PHI, 2014.
4. E. Sanchez-Sinencio and A. G. Andreou, *"Low-Voltage/Low-Power IntegratedCircuits and Systems: Low-Voltage Mixed-Signal Circuits"*, First Edition, John Wiley & Sons, 2015.
5. 4. E. N. Farag and M. I. Elmasry, *"Mixed-Signal VLSI Wireless Design: Circuitsand Systems"*, First Edition, Kluwer Press, 2011.
6. Y. Tsividis, *"Mixed Analog-Digital VLSI Devices and Technology"*, Second Edition, TMH, 2011.

Course Articulation Matrix:

Mixed-Signal Design (ECL-731(i))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	H	H	H	H
CO 2	H	H	H	H	M
CO 3	M	H	H	H	M
CO 4	M	H	M	H	M
CO 5	H	H	H	H	M
CO 6	M	H	M	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

RF Micro-Electronics
ECL-731 (ii)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Analog Electronics

Course Objectives: This Course is for second-year post-graduate students. The objective of this course is to provide students with an understanding of modern RF electronics devices employed in RF Transceiver Design. This course is aimed to provide the knowledge of various issues encountered in high-frequency circuits, such as impedance matching, realization of passive components and bandwidth enhancement. Design components of radio-frequency systems, including low noise amplifiers, oscillators, mixers and power amplifiers will be discussed in detail. The effect of individual components performance on overall radio-frequency transmitter and receiver design and performance are also covered in this course plan.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Define** the basic terminologies related to RF technology and its VLSI implementation.	LOTS: Level 1 Remember
CO 2	**Explain** the working and VLSI implementation of various circuits used in RF systems.	LOTS: Level 2 Understand
CO 3	**Apply** the concept of RF technology in the design of the basic blocks used in RF systems.	LOTS: Level 3 Apply
CO 4	**Analyze** the performance of RF circuits.	HOTS: Level 4 Analyze

Course Contents

UNIT-1

Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology.

Basic concepts in RF Design: Nonlinearly and Time Variance, inter-symbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.

UNIT-2

Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non-coherent defection. Mobile RF Communication systems and basics of Muitiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation.

UNIT-3

Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off, Resonator-less VCO design, Quadrature and single-sideband generators.

UNIT-4

Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques, Design issues in integrated RF filters. Some discussion on available CAD tools for RF VLSI designs.

Reference Books:

1. B. Razavi, "*RF Microelectronics*", Pearson Education, Second Edition, 2012.
2. Thomas Lee, "*The Design of CMOS Radio Frequency Integrated Circuits*", Cambridge University Press, Second Edition, 2004
3. B.Razavi, "*Design of Analog CMOS Integrated Circuits*", First Edition, McGraw Hill, 2001.
4. R.Jacob Baker, "*CMOS Circuit Design Layout and Simulation*", Third Edition, Wiley, 2010.
5. Y.P. Tsividis, "*Mixed Analog-Digital VLSI Devices and Technology*", First Edition, World Scientific, 2002.

Course Articulation Matrix:

RF Micro-Electronics (ECL-731 (ii))					
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**
CO1	H	-	M	H	M
CO2	M	-	H	H	H
CO3	H	L	H	H	H
CO4	H	L	H	H	M

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINNERING

VLSI Testing and Testability
ECL-731 (iii)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: VLSI Design

Course Objectives: This course is introduced to provide the basics of testing techniques for VLSI circuits & to make students understand the various types of faults and fault diagnosis methods. This course also provides the study about the testable memory design and the concepts of the test generation methods.

Course Outcomes:

S.No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Describe** the basic significance of testing which can help them to design a better yield in IC design.	LOTS: Level 1 Remember
CO 2	**Explain** the test generation in sequential and combinational circuits.	LOTS: Level 2 Understand
CO 3	**Demonstrate** the memory test architectures & techniques.	LOTS: Level 3 Apply
CO 4	**Analyze** various trade-offs and techniques for testability.	HOTS: Level 4 Analyze
CO 5	**Design & Develop** more efficient tools from fault coverage and speed point of view.	HOTS: Level 6 Create

Course Contents

UNIT-1

Introduction: The need for testing, the problems of digital and analog testing, Design for test, Software testing Faults in Digital circuits:General introduction, Controllability and Observability. Fault models - Stuck-at faults, Bridging faults, intermittent faults.

UNIT-2

Digital test pattern generation:Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D-algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing.

UNIT-3

Signatures and self-test: Input compression Output compression Arithmetic, Reed-Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients,Spectral coefficients, Coefficienttest signatures, Signature analysis and onlineself-test.

UNIT-4

Testability Techniques: Partitioning and ad hoc methods and Scan-path testing, Boundary scan and IEEE standard 1149.1, Offline built in Self-Test (BIST), Hardware description languages and test

Testing of Analog and Digital circuits: Testing techniques for Filters, A/D Converters, RAM, Programmable logic devices and DSP.

Reference Books:

1. Stanley L. Hurst, *"VLSI Testing: digital and mixed analogue digital techniques"*, First Edition, Inspec/IEEE,1999.
2. Mirron Abramovici, Melvin A. Breuer, Arthur D. Friedman, *"Digital Systems Testing & Testable Design"*, First Edition, Jacio, Publishing House, 2001.
3. P.K.Lala, *"Digital circuit Testing & Testability"*, First edition, Academic Press, 2002.
4. M. Bushnellandand V. Agarwal, *"Essentials of electronic testing for digital, memory & mixed-signal VLSI circuits"*, Kluwer Academic Publisher, 2001 .
5. Vishwani D. Agrawal and Michael L. Bushnell, *"Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits"*, Kluwer Academic Publishers, 2000.
6. L. T. Wang, Cheng Wen Wu and Xiaoqing Wen, *"VLSI Test Principles and Architectures – Design for Testability"*, First Edition, Morgan Kaufmann Publishers, 2006.
7. Robert J. Feugate, Jr. Steven, M. Mentyn, *"Introduction to VLSI Testing"*, PHI, Englehood Cliffs, 1998.

Course Articulation Matrix:

VLSI Testing and Testability (ECL-731(iii))					
	PO1	PO2	PO3	PSO1	PSO2
CO1	H	H	M	M	L
CO2	M	L	H	M	L
CO3	L	L	M	L	M
CO4	M	H	H	M	H
CO5	M	H	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Memory System Design
ECL-731 (iv)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Digital Circuit Design

Course Objectives: This course is for Second year post graduation students. This course is designed for memory system organization, memory technologies, and characterization techniques for memory for low power.

Course Outcomes:

S.No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Define** the concepts and related terminology of memories.	LOTS: Level 1 Remember
CO 2	**Know** the significance of various chip design technologies.	LOTS: Level 2 Understand
CO 3	**Solve** the different problems of DRAM circuits, low power and ultra-low power circuits etc.	LOTS: Level 3 Apply
CO 4	**Solve** problems related to different approaches of memory designing.	HOTS: Level 5 Evaluate
CO 5	**Compile** and Integrate the knowledge of memory designing (RAM, DRAM, High Performance, Low Power, Ultra Low Power etc.) to solve the real world problems.	HOTS: Level 6 Create

Course Contents

UNIT-1

Introduction to Memory Chip Design: Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Basic Operation of The 1-T Cell, Basic Operation of a SRAM Cell, Trends in Non-Volatile Memory Design and Technology, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology,

Basics of RAM Design and Technology: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.

UNIT-2

DRAM Circuits: High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.

UNIT-3

On-Chip Voltage Generators: Substrate-Bias Voltage (VBB) Generator, Voltage Up-Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.

High-Performance Subsystem Memories: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.

UNIT-4

Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.

Ultra-Low-Voltage Memory Circuits: Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low-Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.

Reference Books:

1. K.Itoh, *"VLSI Memory Chip Design"*, First Edition, Springer, 2001.
2. Gerardus Blokdyk, *"Memory Management: A Complete Guide"*, First Edition, 5 STAR Cooks 2021.
3. Roger VillelaIntroducing, *"Mechanisms and APIs for Memory Management: Using Windows OS Native Runtime APIs"*, First Edition, Apress, 2019.
4. DalijaPrasnikar and Neven Prasnikar Jr., *"Delphi Memory Management: For Classic and ARC Compilers"*, First Edition, Create Space Independent Publishing Platform, 2018.
5. David Atienza Alonso, Stylianos Mamagkakis and Christophe Poucet, *"Dynamic Memory Management for Embedded Systems"*, First Edition, Springer, 2014.
6. Francky Catthoor, Sven Wuytack, G.E. de Greef and Florin Banica, *"Custom Memory Management Methodology: Exploration of Memory Organisation for Embedded Multimedia System Design"*, Springer; 1998.

Course Articulation Matrix:

Memory System Design (ECL-731(iv))					
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**
CO1	H	H	M	M	L
CO2	M	L	H	M	L
CO3	L	L	M	L	M
CO4	M	H	H	M	H
CO5	M	H	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Low Power VLSI Design
ECL-731 (v)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Digital System Design, Digital VLSI Design

Course Objectives: This course is meant for the final year post- graduate students. The objective of the course is to provide the students with the understanding of the need for Low power VLSI chips and various sources of power dissipation in the CMOS IC at different abstraction levels.

Course Outcomes:

Sr. No.	At end of the semester,student will be able to	RBT Level
CO 1	**Describe** low power architectures for VLSI design.	LOTS: Level 1 Remember
CO 2	**Explain** the various sources of power dissipation.	LOTS: Level 2 Understand
CO 3	**Apply** the logics power optimization in VLSI design circuits and systems.	LOTS: Level 3 Apply
CO 4	**Analyze** digital system at different abstraction levels for low power design.	HOTS: Level 4 Analyze
CO 5	**Design** digital circuits and systems for low power IC design, test and estimation.	HOTS: Level 6 Create

Course Content

UNIT-1

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power :

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT-2

Power estimation Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT-3

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library Logic level:Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

UNIT-4

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Reference Books:

1. Gary K. Yeap, "*Practical Low Power Digital VLSI Design*", Second Edition, KAP, 2002
2. Rabaey, Pedram, *"Low power design methodologies"* First Edition, Kluwer Academic, 1997
3. Kaushik Roy, Sharat Prasad, *"Low-Power CMOS VLSI Circuit Design"*, Second Edition, Wiley, 2000.
4. Dimitrios Soudris, Christians Pignet, Costas Goutis, *"Designing CMOS Circuits for Low Power"*, First Edition, Kluwer, 2002.
5. J.B.Kulo and J.H Lou, *"Low voltage CMOS VLSI Circuits"*, Second Edition, Wiley 1999.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, *"Low power digital VLSI design"*, Second Edition, Kluwer, 1995.

Course Articulation Matrix:

Low Power VLSI Design (ECL-731(v))					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	M	H	M	H	H
CO 2	M	H	M	H	M
CO 3	H	H	H	H	M
CO 4	M	H	H	H	M
CO 5	L	M	H	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Wireless Sensor Networks

ECL-731 (vi)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Wireless Communication and Computer Networks

Course Objectives: This elective course is a blend of the concepts developed in the core courses like wireless mobile communication and computer networks. This course is aimed todevelop the basic understanding and impart in-depth knowledge of various topics like wireless sensor network architecture, protocols & its establishment.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to	RBTLevel
CO 1	**Outline** the terminology, general architecture and application areas of wireless sensor networks.	LOTS: Level 1 Remember
CO 2	**Explain** the working of WSNs with the help of various MAC, routing and transport control protocols.	LOTS: Level 2 Understand
CO 3	**Apply** the knowledge gained to address the design issues and challenges involved in wireless sensor networks.	LOTS: Level 3 Apply
CO 4	**Analyze** the working and performance of various WSN protocols and systems.	HOTS: Level 4 Analyze

Course Content

UNIT-1

Introduction: Architectural Elements, Basic Technology, Sensor Node, Hardware and Software, Sensor Taxonomy, Design challenges, Characteristics and requirements of WSNs, Applications.

UNIT-2

MAC Protocols for WSN: Fundamentals of MAC Protocols, Performance Requirements, Common Protocols, MAC for WSN, Schedule based protocols, Random Access based Protocols, Sensor-MAC, IEEE802.15.4 LR-WPAN's Standard

UNIT-3

Routing Protocols for WSN: Data Dissemination and Gathering, Challenges and Design Issues, Network Scale and TimeVarying Characteristics, Routing Strategies, Flooding and its variants.

UNIT-4

Transport Control Protocols for WSN: Design Issues, Congestion Detection and Avoidance, Event-to-Sink Reliable Transport, Reliable Multi-segment Transport; Pump Slowly, Fetch Quickly, GARUDA, ATP, Congestion and Packet Loss Recovery.
WSN Infrastructure Establishment: Topology Control, Clustering, Time Synchronization, localization and positioning, Sensor Tasking and Control.

Reference Books:

1. K. Sohraby, Minoli, and T. Znati, *"Wireless Sensor Networks: Technology, Protocolsand Applications"*, John Wiley and Sons, 2007.
2. H. Karl and A. Willig, *"Protocols and Architectures for Wireless Sensor Networks"*, John Wiley and Sons, 2007.
3. C.S. Raghavendra, K.M. Sivalingam and T. Zanti, *"Wireless Sensor Networks"*, Springer Verlag, Sep. 2006.
4. W. Dargie, C. Poellabauer, *"Fundamentals of Wireless Sensor Networks: Theory and Practice,"* John Wiley & Sons, 2010.
5. E.H. Callaway Jr., *"Wireless Sensor Networks: Architectures and Protocols"*, Auerbach Publications, CRC Press, 2004.

Course Articulation Matrix:

Wireless Sensor Networks (ECL-731 (vi))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO1	-	-	L	L	L
CO2	L	-	M	H	L
CO3	L	-	H	H	M
CO4	M	-	H	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Advanced Digital Communication
ECL-731 (vii)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Communication system

Course Objectives: This subject aims to develop a thorough understanding of the main concepts, techniques and performance criteria used in the analysis and design of digital communication systems.

Topics include:-

1. Introduction of digital communication system.
2. Digital modulation techniques.
3. Reception of digital signal.
4. Information theory and coding.

Course Outcomes:

S.No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Describe** the basic significance of various factors in design of digital communication system.	LOTS: Level 1 Remember
CO 2	**Explain** the transmitter & receiver structure of various digital communication system	LOTS: Level 2 Understand
CO 3	**Demonstrate** the performance of digital communication systems based on various modulation techniques.	LOTS: Level 3 Apply
CO 4	**Analyze** modulation techniques used in a modern digital communication system.	HOTS: Level 4 Analyze
CO 5	**Design** advanced digital communication systems using modulation techniques and coding.	HOTS: Level 6 Create

Course Content

UNIT-1

Introduction: Elements of Digital Communication system, Bandpass and Lowpass signal representation, Comparison between analog &digital communication, Performance parameters of Digital Communication, Concept of Constellation, BER, etc.

UNIT-2

Digital Modulation Techniques: Representation of Digitally Modulated signal, Memoryless modulation method: pulse amplitude modulation, phase modulation, Quadrature Amplitude modulation; Memory based modulation methods: Continuous Phase Frequency-Shift Keying, Continuous Phase Modulation.

UNIT-3

Reception of Digital Signal: Baseband signal reception, Probability of error, Optimum filter receiver, Matched filter receiver, Coherent reception, calculation of error probability for PSK, MSK, ISI.

UNIT-4

Communication Link Analysis: Channel: error-performance degradation, Sources of signal loss and noise; the range equation of received signal power and noise power, received signal power and path loss in terms of frequency, Link Budget analysis, link budget calculation in decibels, link margin, Link availability, Link budget details, system Trade-offs.

Reference Books:

1. J.G Proakis and M Salehi, "*Digital Communications*", Fifth Edition, TataMcGraw Hill, 2008.
2. H. Taub and D. L. Schilling, "*Principle of Communication systems*", Third Edition, TataMcGraw Hill, 2011.
3. S. Haykin, "*Digital Communications*", Fourth Edition, John Wiley & Sons, 2001.
4. B. Sklar and P. K. Ray, "*Digial Communications – Fundamentals and Applications*", Second Edition, Pearson, 2001.
5. B.P.Lathi,"*Modern Digital and Analog Communication Systems*", Fifth Edition, Oxford University Press, 2019.

Course Articulation Matrix:

Advanced Digital Communication (ECL-731 (vii))					
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**
CO 1	H	H	M	M	L
CO 2	M	L	H	M	L
CO 3	L	L	M	L	M
CO 4	M	H	H	M	H
CO 5	M	H	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Satellite Communication
ECL-731 (viii)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Communication System

Course Objectives: Satellite Communication Systems play a vital role in the global telecommunication system. It provides an essential and economical fixed and mobile communication services over broad coverage areas of land, sea and air. The course goal for Satellite Communications is to provide the student with the basic understanding and an in-depth knowledge of various concepts used in a satellite communication system. In this course, you will learn the about the science behind the orbiting satellites, link design and calculation, various multiple access schemes and earth station parameters used for satellite communication. In the end various applications of satellite communication will be discussed.

Course Outcomes:

Sr. No.	At end of the semester, students will be able to	RBT Level
CO 1	**Describe** terminologies & various terms of satellite communication systems.	LOTS: Level 1 Remember
CO 2	**Generalize** various applications of satellite communication systems.	LOTS: Level 2 Understand
CO 3	**Demonstrate** the concepts of space segment and earth segment in satellite communication systems.	LOTS: Level 3 Apply
CO 4	**Compare** the performance of various multiple access techniques in satellite communication.	HOTS: Level 4 Analyze
CO 5	**Design** basic link design equation based on the various parameters.	HOTS: Level 6 Create

Course Content

UNIT-1

Basics of Satellite Communication:
Overview of Satellite Systems, Frequency Allocations for Satellite Services, Orbits and Launching Methods, Orbital Elements, Inclined Orbits, The Geostationary Orbit, Antenna Look Angles, Limits of Visibility, Launching Orbits.

UNIT-2

The Space Segment & Earth Segment:
The Power Supply, Attitude & Thermal Control, Station Keeping, TT&C Subsystem, Transponders, Receive-Only Home TV.

The Space Link:
Link-Power Budget Equation, System Noise, Carrier-to-Noise Ratio, Input back-off, Output back-off, Effects of Rain, Combined Uplink and Downlink *C/N* Ratio.

UNIT-3

Access Techniques:
FDMA, Spade System, TDMA, On-Board Signal Processing for FDMA/TDM Operation, Satellite-Switched TDMA, Code-Division Multiple Access.

UNIT-4

Satellite Applications:
Direct Broadcast Satellite (DBS) Television, High Definition Television (HDTV), Satellite Mobile Services, VSATs, Radarsat, Global Positioning Satellite System (GPS), Orbcomm.

Reference Books:

1. D. Rody, *"Satellite Communication"*, Fourth Edition, Prentice Hall, 1983.
2. Tri T.Ha, *"Digital Satellite Communication"*, Second Edition, McGraw Hill, 1990.
3. K. Feher, *"Digital Communication Satellite / Earth Station Engineering"*, Prentice Hall, 1983.
4. Bruce R. Elbert, *"The Satellite Communication Applications Hand Book"*, Artech House, 1997.
5. W. L. Pritchard, H. G. Suyder hood, R. A. Nelson, *"Satellite Communication Systems Engineering"*, Second Edition, Prentice Hall, 1993.

Course Articulation Matrix:

Satellite Communication (ECL-731 (viii))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	H	H	H	M
CO 2	M	L	H	H	H
CO 3	M	L	H	M	H
CO 4	M	M	H	H	H
CO 5	M	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

FPGA Design
ECL-731(ix)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. it will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Digital System Design, Hardware Description Languages

Course Objectives: The course provides an overview of FPGA VLSI Design, particularly for arithmetic logic and systems and deals with both the function of related components and system performance. The classification and requirements of FPGA for design automation, HDL design, synthesis for FPGA and ASIC design with practical implementation are demonstrated.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO 1	**Describe** the concept of HDL and digital design flow for electronic circuits and systems and their technical specifications.	LOTS: Level 1 Remember
CO 2	**Understand** various HDL features and capabilities for circuits and systems design.	LOTS: Level 2 Understand
CO 3	**Apply** the concepts of FPGA for design of digital logics in the integrated circuits and systems.	LOTS: Level 3 Apply
CO 4	**Analyze** digital system at different abstraction levels.	HOTS: Level 4 Analyze
CO 5	**Evaluate** digital system at different abstraction levels.	HOTS: Level 5 Evaluate
CO 6	**Design** digital circuits and systems for IC design, test and verification in the arithmetic functions, digital signal processing, etc.	HOTS: Level 6 Create

Course Content

UNIT-1

Digital system design automation with Verilog, digital design flow, ASICs, FPGAs, Architectures of XILINX and ALTERA FPGA devices, hardware modelling with Verilog, System Verilog, RTL Level design with Verilog-architecture based coding in Verilog, design example for architecting speed, power and area in Verilog for FPGA design. High level design, design abstractions, Processor, Memory, Arrays, state machines, DSP Design, clock domains.

UNIT-2

FPGA in arithmetic circuits, implementation of math functions, floating point unit design, microprocessor design, FPGA applications in DSP, image processing, speech processing, audio processing, information system, instrumentation and control system, computer system vision, machine learning, artificial intelligent, Reconfigurable design and architectures.

UNIT-3

Coding for synthesis, Efficient resource utilization, Constrains based synthesis, False paths and multi cycle paths, constraint file creation, Gate level simulation, high-level synthesis, Floor Planning, placement, Back annotation, SDF Format, hardware testing and design for testability,

fault models, fault coverage, ATPG, functional tests, types of DFT, Scan insertion, BIST, verification and verification methodologies.

UNIT-4

Industry Standard FPGA and ASIC design tools, FPGA Design flows, IP generator, System generator, memory controller, Scripting and customization of tool environment, simulation, synthesis, clocking, timing and power analysis, timing closure, hardware debug.

Reference Books:

1. Z. Navabi, *"Verilog Digital System Design"*, Second Edition, McGraw Hill, 2015.
2. Steve Kilts, *"Advanced FPGA Design-Architecture, Implementation, and Optimization"*, Second Edition, Wiley, 2007.
3. Hong Jeong, *"Architectures for Computer Vision from Algorithm to Chip with Verilog"*, First Edition, Wiley, 2014.
4. Sanjay Churiwala, *"Designing with Xilinx FPGAs-Vivado"*, First Edition, Springer, 2017.
5. Uwe Meyer-Baese, *"Signal and Communication Technology-Digital Signal Processing with Field Programmable Gate Arrays"*, Fourth Edition, Springer, 2014.
6. M. Morris Mano, Michael D. Ciletti, *"Digital Design with an Introduction to the Verilog HDL, VHDL, and SystemVerilog"*, Sixth Edition, Pearson Education, 2018.

Course Articulation Matrix:

FPGA Design (ECL-731(ix))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	H	H	H	H
CO 2	H	H	H	H	M
CO 3	H	H	H	H	M
CO 4	M	H	H	H	M
CO 5	H	H	H	H	M
CO 6	H	H	H	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Advanced Antenna Theory and Design
ECL-731(x)

General Course Information

Course Credits: 3 Type: Elective Contact Hours: 3 hours/week Mode: Lectures (L) Examination Duration: 3 hours	**Course Assessment Methods; Max. Marks: 100 (Internal: 30; External: 70)** Three minor tests, each of 20 marks, will be conducted. The third minor will be conducted in open book mode by the Course Coordinator. No date sheet will be issued for the third minor at the level of the Departments. For the purpose of internal assessment, the average of the highest marks obtained by a student in any two minor examinations will be considered. All the minor examination question papers will be prepared and evaluated by following the Outcome Based Education framework. Class Performance will be measured through percentage of lectures attended (4 marks) Assignments (4 marks) and class performance (2 marks). The end semester examination will be of 70 marks. For the end semester examination, nine questions are to be set by the examiner. Question number one will be compulsory and based on the entire syllabus. It will contain seven short answers type questions. Rest of the eight questions is to be given by setting two questions from each of the four units of the syllabus. A candidate is required to attempt any other four questions selecting one from each of the four units. All questions carry equal marks

Pre-requisites: Electromagnetic theory, antenna and wave propagation

Course Objective: This course is for second year post graduation students. The course objective is to understand the theory and fundamentals of antenna design. The course helps the students to learn key aspects of practical antenna design. A broad range of antennas such as dipole, loop, microstrip patch, horn, etc are studied during the course.

Course Outcome:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Memorize and define** standard antenna characterization parameters such as: impedance, far-field radiation pattern, scattering pattern, gain, directivity, bandwidth, beam width, polarization, and efficiency.	LOTS: Level1 Remember
CO 2	**Explain** the basics and theory behind antenna radiation mechanisms, point sources, small-wave dipoles, half-wave dipoles, and the fundamentals of antenna measurements.	LOTS: Level 2 Understand
CO 3	**Apply** the fundamental knowledge gained about electromagnetic radiation mechanism and its physics and be able to **examine** radiation from several common antenna structures.	LOTS: Level 3 Apply
CO 4	**Analyze** the requirements and potential design options for different antenna applications.	HOTS: Level 4 Analyze
CO 5	**Evaluate** the performance characteristics of antennas using different performance parameters.	HOTS: Level 5 Evaluate
CO 6	**Design** antennas such as dipoles, microstrip patches, horns and antenna arrays to achieve specified performance.	HOTS: Level 6 Create

Course Content

UNIT -1

Antenna Fundamentals: Fundamentals of electromagnetics, the ideal dipole, radiation patterns, directivity and gain, antenna impedance, radiation efficiency, antenna polarization.
Simple radiating elements: half wave dipoles, monopoles, loop antennas, two element arrays.
System applications for antennas: Receiving properties of antennas, antenna noise and radiometry, antennas in wireless communication systems, antennas in radar systems.

UNIT-2

Broadband Antennas: Travelling wave wire antennas, helical antennas, biconical antennas, sleeve antennas, spiral antennas, wideband EMC antennas, Ultra-wideband antennas.
Aperture Antennas: Radiation from apertures and Huygens' principle, rectangular apertures, rectangular horn antennas, circular apertures, reflector antennas, feed antennas for reflectors, Lens antenna.
Horn Antennas: E-Plane, H-plane Sectoral horns, Pyramidal and Conical horns.

UNIT-3

Low-Profile Antennas and Personal Communication Antennas: Introduction, Microstrip antenna elements: Rectangular microstrip patch antennas, other microstrip patch antennas and their applications, broadband microstrip patch antennas, microstrip arrays, microstrip leaky

wave antennas: characteristics of leaky wave antennas, microstrip modes, propagation regimes.

Antennas for Compact Devices: Normal mode helix type antennas, planar Inverted-F Type antennas, other compact antennas, multiband/broadband handset antennas, radio frequency identification (RFID) antennas, Dielectric resonator antennas.

UNIT-4

Antenna Measurements: Reciprocity and antenna measurements, Antenna Ranges, Radiation Patterns, Gain Measurements, Directivity Measurements, Radiation Efficiency, Impedance Measurements, Current Measurements, Polarization Measurements, Human body effect on antenna performance, radiation hazards.

Reference Books:

1. C. A. Balanis, *"Antenna Theory Analysis and Design"*, Fourth Edition, John Wiley & Sons, 2016.
2. W. L. Stutzman and G. A. Thiele, *"Antenna Theory and Design"*, Third Edition, John Wiley & Sons, 2013.
3. J. D. Kraus and R. J. Marhefka, *"Antennas for All Applications"*, First Edition, TataMcGraw-Hill, 2003.
4. J. L. Volakis, *"Antenna Engineering handbook"*, Fifth Edition, TataMcGraw-Hill, 2019.
5. R. Garg, P. Bhartia, I. J. Bahl, A. Ittipiboon, *"Microstrip Antenna Design Handbook"* First Edition, Artech house, 2001.

Course Articulation Matrix:

Advanced Antenna Theory and Design (ECL-731(x))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	-	L	M	L
CO 2	M	M	M	H	M
CO 3	M	M	M	H	H
CO 4	H	M	H	H	H
CO 5	H	M	H	H	H
CO 6	H	M	M	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Advance VLSI Design Lab
ECP-732

General Course Information

Course Credits: 2 Contact Hours: 4/week (L-T-P: 0-0-4) Mode : Lab Work	**Course Assessment Methods (Internal: 50; External: 50)** The internal and external assessment is based on the level of participation in laboratory sessions, timely submission of experiments/assignments, the quality of solutions designed for the assignments, the performance in VIVA-VOCE, the quality of laboratory file and ethical practices followed. There will be a continuous process for laboratory course evaluation. Two internal examinations (each of 50 marks) for the laboratory courses (Minor Laboratory Evaluations: MLE I and MLE II) will be conducted in the week before or after the internal examinations for the theory courses. The overall internal marks will be calculated as the average of the two minor laboratory course evaluations. The course coordinator will conduct these minor evaluations in the slots assigned to them as per their timetable. The Chairperson of the Department will only notify the week for the internal laboratory course evaluations. The marks for MLE I and MLE II must be submitted within a week of the conduct of these laboratory course evaluations. The external examination will be conducted by external examiner appointed by the Controller of Examination along with the internal examiner, preferably the lab course coordinator, appointed by the Chairperson of the Department. The final practical examination of duration three hours will be conducted only in groups of 20-25 students. The Course Coordinator / Internal Examiners/ External Examiners will maintain and submit the bifurcation of marks obtained by the students in their respective internal/external evaluations in the specified proformas (attached herewith as Annexures I and II) to the respective departments in addition to the submitting and uploading of overall marks on the university portal as per the requirement of the result branch. The laboratory course coordinator will also conduct laboratory course exit survey and, compute and submit the attainment levels of the laboratory course based on direct and indirect evaluation components and submit it to the Chairperson office along with the internal assessment marks.

Pre-requisites: Analog Electronics, Digital VLSI Design

Course Objective: This course is for first year post graduation students. This course is designed to give students in hand practice of writing and simulating a Verilog code which is one of the popular hardware descriptive language. Various combinational and sequential circuits like simple logic gates, Half Adder, Full Adder, Multiplexer, Demultiplexer, Encoder, decoder, Flip-Flops, Shift Register, Counters are included.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO 1	**Understand** CAD tools and technologies for VLSI logic, gates, circuits and systems for Analog, Digital and AMS	LOTS: Levels 3 Apply
CO 2	**Compare** the outcomes of different experimental models of Analog, Digital and AMS systems.	HOTS: Level 4 Analysc
CO 3	**Evaluate** the performance of logics design and verification of Analog, Digital and AMS systems.	HOTS: Level 5 Evaluate
CO 4	**Integrate** knowledge for design of digital circuits and systems for VLSI design, test and verification.	HOTS: Level 6 Create
CO 5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO 6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

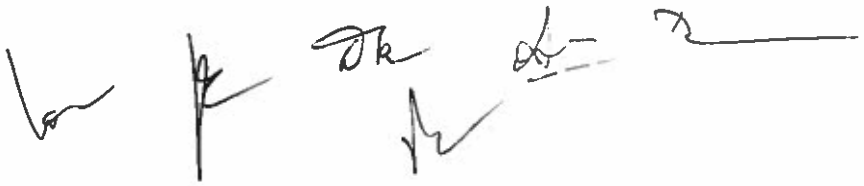
List of Experiments

1. Design and simulate the CMOS Inverting amplifiers stages.
2. Design and simulate the layout of CMOS inverter.
3. Design of various current-mirror circuits.
4. Design a differential pair circuit.
5. Design an operational transconductance ampiifier.
6. Design a three-stage operational amplifier.
7. Design Analog to Digital Converter circuit(s)
8. Design Digital to Analog Converter circuit(s)
9. Design Voltage control oscillator (VCO)

Note: At least eight experiments are to be performed in the semester, out of which atleast six experiments should be performed from the given list. The remaining two experiments may either be performed from the list or designed & setup by the concerned institution as per the scope of the syllabus.

Course Articulation Matrix:

Advance VLSI Design Lab (ECP-732)					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	H	M	H	H	H
CO 2	H	M	H	H	H
CO 3	H	M	H	H	H
CO 4	H	M	M	H	M
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Communication System Design Lab
ECP-733

General Course Information

Course Credits: 2 Contact Hours: 4/week (L-T-P: 0-0-4) Mode : Lab Work	**Course Assessment Methods (Internal: 50; External: 50)** The internal and external assessment is based on the level of participation in laboratory sessions, timely submission of experiments/assignments, the quality of solutions designed for the assignments, the performance in VIVA-VOCE, the quality of laboratory file and ethical practices followed. There will be a continuous process for laboratory course evaluation. Two internal examinations (each of 50 marks) for the laboratory courses (Minor Laboratory Evaluations: MLE I and MLE II) will be conducted in the week before or after the internal examinations for the theory courses. The overall internal marks will be calculated as the average of the two minor laboratory course evaluations. The course coordinator will conduct these minor evaluations in the slots assigned to them as per their timetable. The Chairperson of the Department will only notify the week for the internal laboratory course evaluations. The marks for MLE I and MLE II must be submitted within a week of the conduct of these laboratory course evaluations. The external examination will be conducted by external examiner appointed by the Controller of Examination along with the internal examiner, preferably the lab course coordinator, appointed by the Chairperson of the Department. The final practical examination of duration three hours will be conducted. The Course Coordinator / Internal Examiners/ External Examiners will maintain and submit the bifurcation of marks obtained by the students in their respective internal/external evaluations in the specified proformas (attached herewith as Annexures I and II) to the respective departments in addition to the submitting and uploading of overall marks on the university portal as per the requirement of the result branch. The laboratory course coordinator will also conduct laboratory course exit survey and, compute and submit the attainment levels of the laboratory course based on direct and indirect evaluation components and submit it to the Chairperson office along with the internal assessment marks.

Pre-requisites: Communication System

Course Objectives: The course provides an overview of optical communication, particularly fiber optics and deals with both the function of related components and system performance. Various fiber impairments including linear & non-linear effects are investigated in terms of different metrices like BER, Q factor, eye diagram etc.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able:	RBT Level
CO 1	**Identify** software tools and apply these tools to simulate different optical links.	LOTS: Levels I Remember
CO 2	**Analyze** the outcomes of designed optical networks.	HOTS: Level 4 Analyse
CO 3	**Evaluate** the performance of developed optical links against different limitations of optical fiber transmission.	HOTS: Level 5 Evaluate
CO 4	**Combine** knowledge for design of different types of optical links using various optical components for long haul quality transmission.	HOTS: Level 6 Create
CO 5	Create written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO 6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

List of Experiments

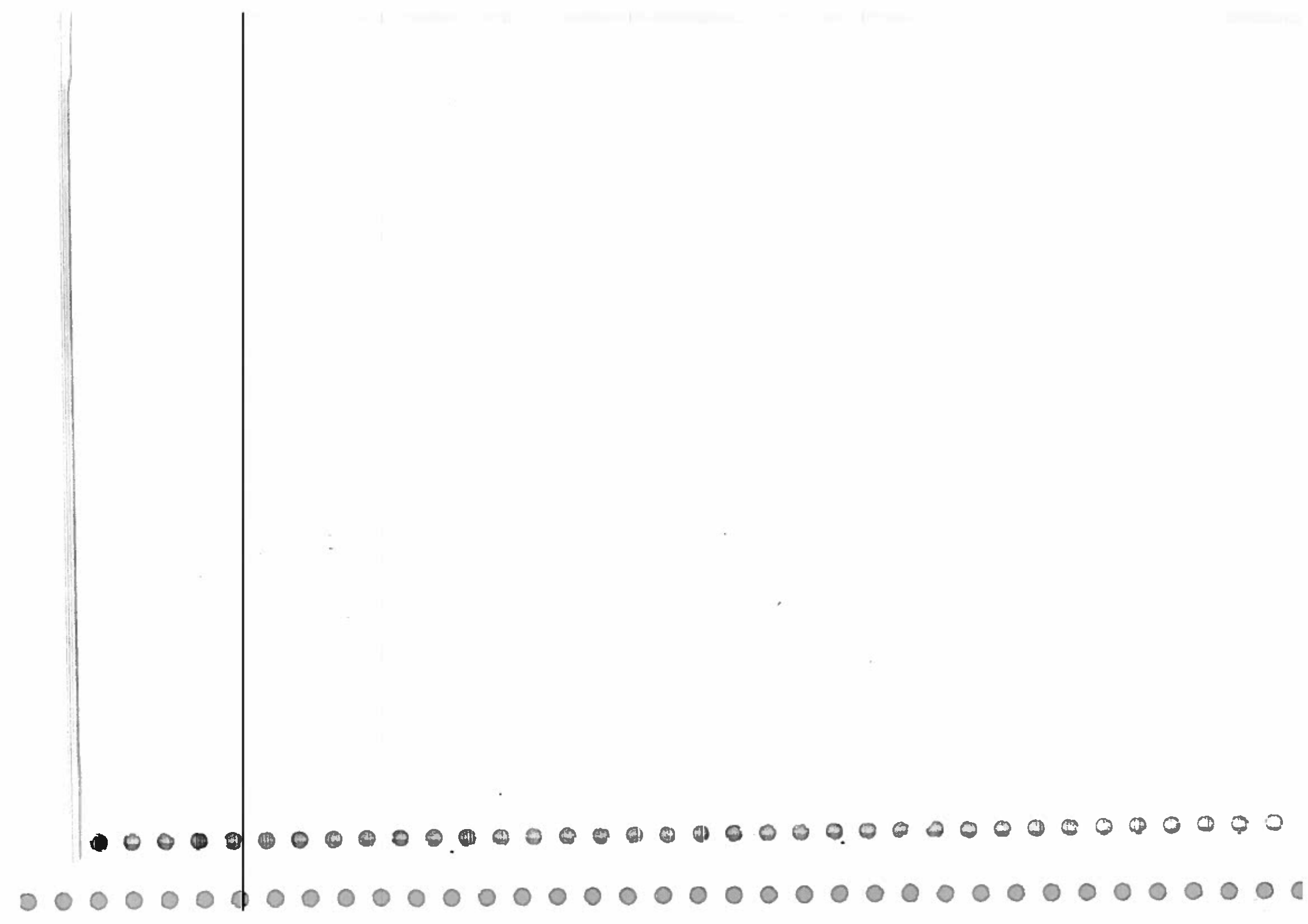
1. To study dispersion in optical links, with and without compensation.
2. To study four channels WDM using computer system using two spans of dispersion shifted fiber of opposite dispersion value.
3. To study fiber linear effects (Polarization mode dispersion).
4. To study self-phase modulation by establishing an optical link.
5. To study cross phase modulation (XPM)by establishing an optical link.
6. To study Stimulated Raman Scattering (SRS) effect by establishing a WDMoptical link.

7. To study Four Wave Mixing (FWM) by establishing aWDMoptical link.
8. To design an optical link of 100 km length and to evaluate BER & Q factor.
9. To design DQPSK modulated optical communication link using RZ, NRZ & duo binary technique.
10. To design an optical fiber transmission link in the presence of combined non linear effects.

Note: Students are required to perform eight to ten experiments in the semester. The above list is an indicative list of experiments, which can be expanded by course coordinator depending on the course requirement.

Course Articulation Matrix:

Communication System Design Lab (ECP-733)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	L	M	H	H
CO 2	H	L	H	H	M
CO 3	H	M	H	H	H
CO 4	H	M	H	H	H
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Dissertation-Part I
ECD-730

Course Code	Title of course	Core/Elective	Credit	L	P
ECD-730	Dissertation-Part I	Core	3	0	*
Max Marks: 100 (Evaluation will be done internally by the dept. including the supervisor concerned)					

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Knowledge of research area

Course Objective: The objective of this course is to make students capable of carrying out detailed literature review in the respective research area. The students should be able to identify research issues, gaps in the literature and thus formulate the specific research problem.

Course Outcomes:

Sr. No.	At the end of the semester students will be able to:	RBTLevel
CO 1	**Summarize** the findings of research papers related to a topic and identify the gaps through extensive literature survey.	LOTS: Level 2 Understand
CO 2	**Use** different modern hardware and software tools to carry out research in the domain of ECE.	LOTS: Level 3 Apply
CO 3	**Analyze** the existing researchcritically to formulate the research problem.	HOTS: Level 4 Analyze
CO 4	**Compile** research ideas in theform of asynopsis/report and present them in an effective manner.	HOTS: Level 6 Create

The dissertation work should be of Research nature only and it should be started during the thirdsemester and the candidate must do the following:

a) Literature Survey
b) Problem Formulation

Around 40% of the dissertation work should be completed in this semester. The remaining 60% work will be carried out in the fourth semester. Each student is required to submit a detailed report about the work done on topic of dissertation as per the guidelines decided by

the department. The dissertation work is to be evaluated internally through Presentations during the semester and Viva-Voce at the end of semester as per the guidelines decided by the department from time to time.

***2 hrs per student per week teaching load will be assigned to supervisor.**
Mode: One-to-one discussions with the Supervisor.

Course Articulation Matrix:

Dissertation–Part I (ECD-730)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	L	H	H	-
CO 2	H	-	H	H	H
CO 3	H	-	H	H	H
CO 4	M	H	-	-	-

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Seminar
ECP-735

Course code	Title of course	Core/Elective	Credit	L	P
ECP-735	Seminar	Core	1	0	2
Max. Marks: 100		Internal: 100 Marks			

Course Assessment Methods: Both Continuous & Semester End Assessment

Course Objectives: This course is introduced for the students to learn fundamental principles, concepts or theories and to identify & compare technical and practical issues related to the area of specialization.It also motivates the students to prepare a well-organized report employing elements of technical writing and critical thinking for promotion and development of presentation skills.

Course Outcomes:

S.No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Describe** any topic of interest and develop a thought process for technical presentation.	LOTS: Level 1 Remember
CO 2	**Explain** technical issues and give oral presentations related to the work completed.	LOTS: Level 2 Understand
CO 3	**Demonstrate** ability to use technical resources available.	LOTS: Level 3 Apply
CO 4	**Compare** technical issues and develop competence in presenting.	HOTS: Level 5 Evaluate
CO 5	**Develop** their communication skills.	HOTS: Level 6 Create

Course Articulation Matrix:

Seminar (ECP-735)					
	PO1	**PO2**	**PO3**	**PSO1**	**PSO2**
CO1	H	M	M	M	L
CO2	H	H	M	L	M
CO3	H	L	L	M	H
CO4	H	H	M	M	M
CO5	H	M	M	L	L

Fourth Semester

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Dissertation–Part II
ECD-740

Course Code	Title of course	Core/Elective	Credit	L	P
ECD-740	Dissertation–Part II	Core	8	0	*
Max Marks: 100 (The evaluation will be done by external exam conducted jointly by the external examiner and the supervisor concerned as internal examiner.)					

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Knowledge of research area

Course Objective: The main objective of this course is to make students capable of carrying out research / investigation and development work independently to solve practical problems. Further, it is also aimed to develop solution oriented understanding and higher degree of mastery in the specialized area of electronics and communication engineering.

Course Outcomes:

Sr. No.	At the end of the semester students will be able to:	RBTLevel
CO1	**Apply** advanced concepts, research methodology and knowledge of simulation tools to solve the research problem.	LOTS: Level 3 Apply
CO2	**Analyze** research objectives critically and explore a logical solution through experimentation / simulation for the proposed research work.	HOTS: Level 4 Analyze
CO3	**Evaluate** the experimentation / simulation results of the proposed research.	HOTS: Level 5 Evaluate
CO4	**Devise** a novel & effective solution to the research problem and write dissertation/papers in a professional and ethical manner.	HOTS: Level 6 Create

Around 40% of the dissertation work should be completed in third semester. The remaining 60%work will be carried out in this semester. Each student is required to submit a detailed Dissertation report of the work done (III Sem + IV Sem) on topic of Dissertation as per the guidelines decided by the department.

The Dissertation work is to be evaluated continuously through presentations during the semester. The candidate will be required to present his/her research work before submitting his/her Dissertation (pre-submission) in front of dept. committee including Chairperson of the

department. Final dissertation evaluation/ viva voce will be done at the end of semester as per the guidelines decided by the department/university from time to time.

The candidate has to present/publish one paper in national/international conference/ symposium/journalbefore the submission of Dissertation. Research work should be carried out at GJUS&T Hisar. However, candidate may visit research labs/institutions with the due permission of Chairperson on recommendation of supervisor concerned.

***02 hrs per student per week teaching load will be assigned to supervisor.**
Mode: One-to-one discussions with the Supervisor.

Course Articulation Matrix:

Dissertation–Part II (ECD-740)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	-	H	H	H
CO 2	H	-	H	H	H
CO 3	H	M	H	H	H
CO 4	H	H	H	H	H

Annexure-I

Office of the Dean Faculty of Engineering and Technology

Hisar-125001

(Established by State Legislative Act 17 of 1995)

'A' GRADE NAAC Accredited

Guru Jambheshwar University of Science and Technology

Faculty of Engineering and Technology
Guru Jambheshwar University of Science and Technology, Hisar-125001

Internal Laboratory Course Evaluation Proforma

Minor Laboratory Course Evaluation-I (MLE-I) / Minor Laboratory Course Evaluation-II (MLE-II)

Name of the Programme:
Semester:
Nomenclature of the Course:
Course Code:

SR. No.	Roll. No.	Written work and /or Conduct of Experiment(s)	(VIVA-VOCE) based on laboratory Course Outcomes CO-2 to CO-4			Laboratory Record/File	Class Performance (Attendance/Ethical practices followed, Self-Learning and Team Spirit)	Total Marks
		CO-1 (15)	CO-2 (5)	CO-3 (5)	CO-4 (5)	CO-5 (10)	CO-6 (10)	50
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
Total No. of Students:			Present:			Absent		

Name of the Course Coordinator	Signature of the Course Coordinator

Annexure-II

Office of the Dean Faculty of Engineering and Technology
Guru Jambheshwar University of Science and Technology Hisar-125001
(Established by State Legislative Act 17 of 1995)'A' GRADE NAAC Accredited

Faculty of Engineering and Technology
Guru Jambheshwar University of Science and Technology, Hisar-125001

External Laboratory Course Evaluation Proforma

Nomenclature of the Course:
Course Code:
Name of the Internal Examiner:
Name of the External Examiner:

SR. No.	Roll. No.	Conduct of Experiment(s) (20)	(VIVA-VOCE) (20)	Laboratory Record/Practical write up (10)	Total Marks (50)
1					
2					
3					
.4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Total No. of Students:	Present:	Absent:
Signature of the Internal Examiner Name of the Internal Examiner	Signature of the External Examiner Name of the External Examiner	